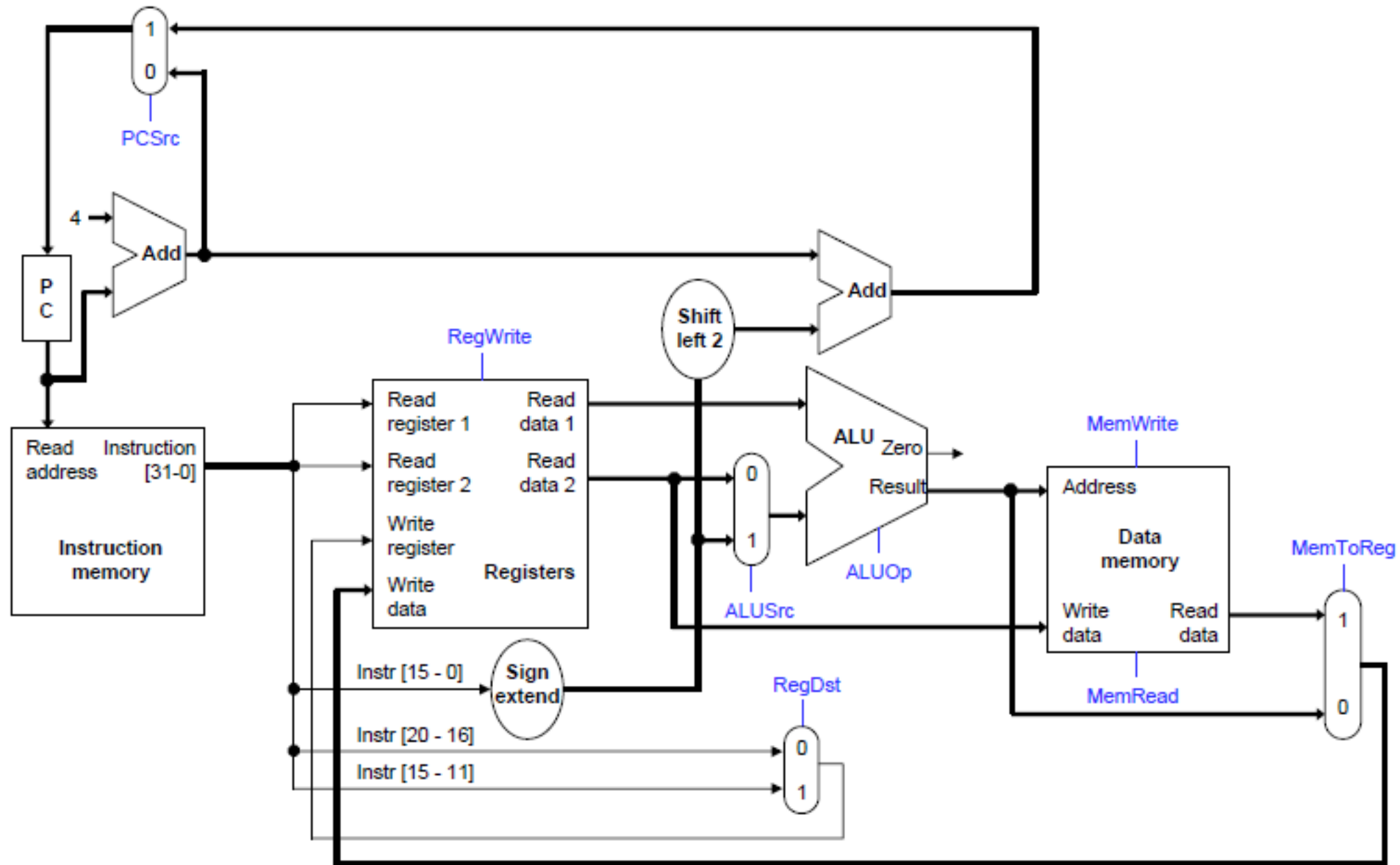*Saeed Safari*

MIPS – Pipeline

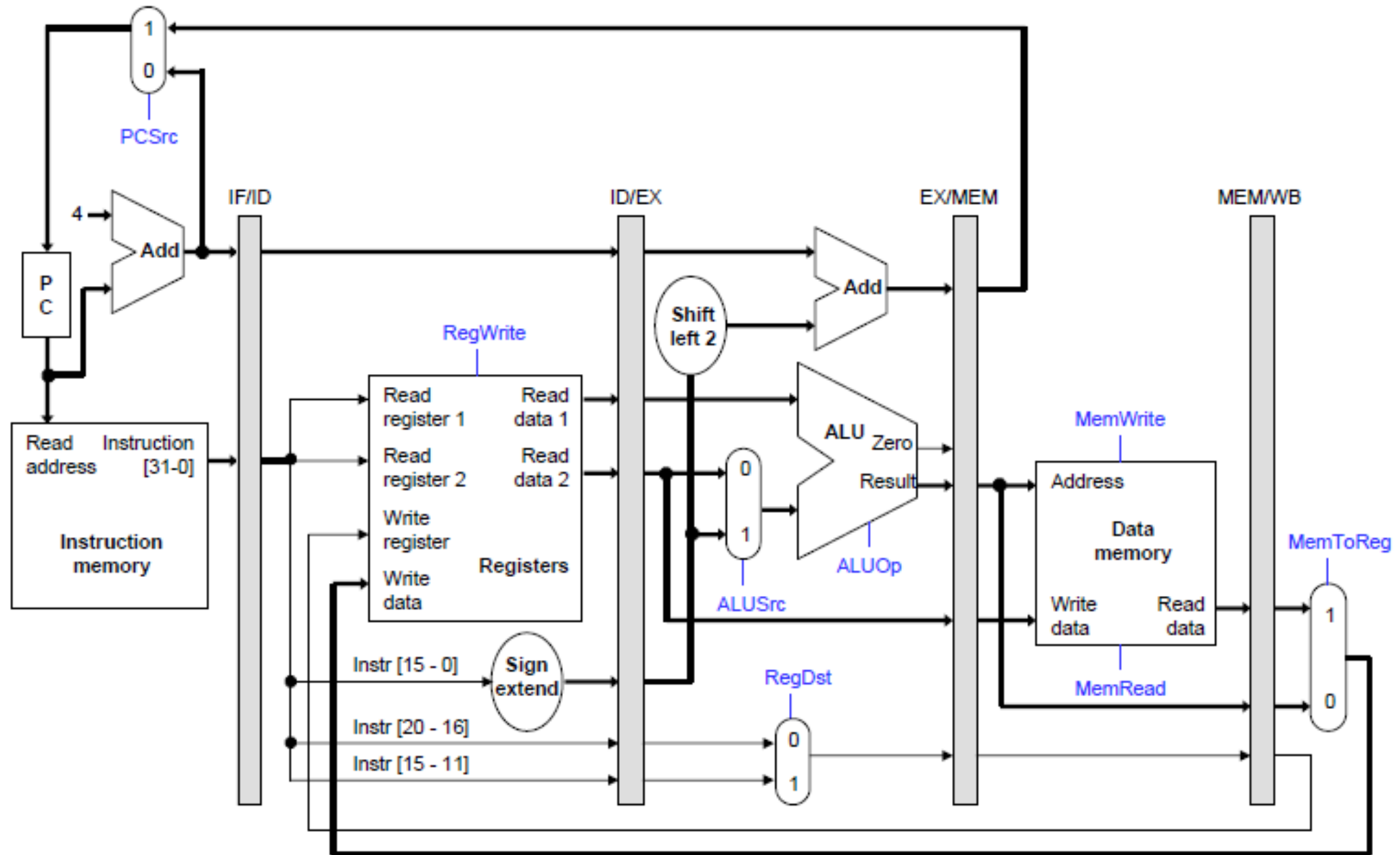ECE School,
Faculty of Engineering,
University of Tehran

Outline

- **Pipeline Processor**
  - **Pipelined Datapath**
  - **Pipelined Controller**
- **Data Hazard**
  - **Data Forwarding**
  - **Pipeline Stall**
- **Control Hazard**
  - **Branch Prediction**

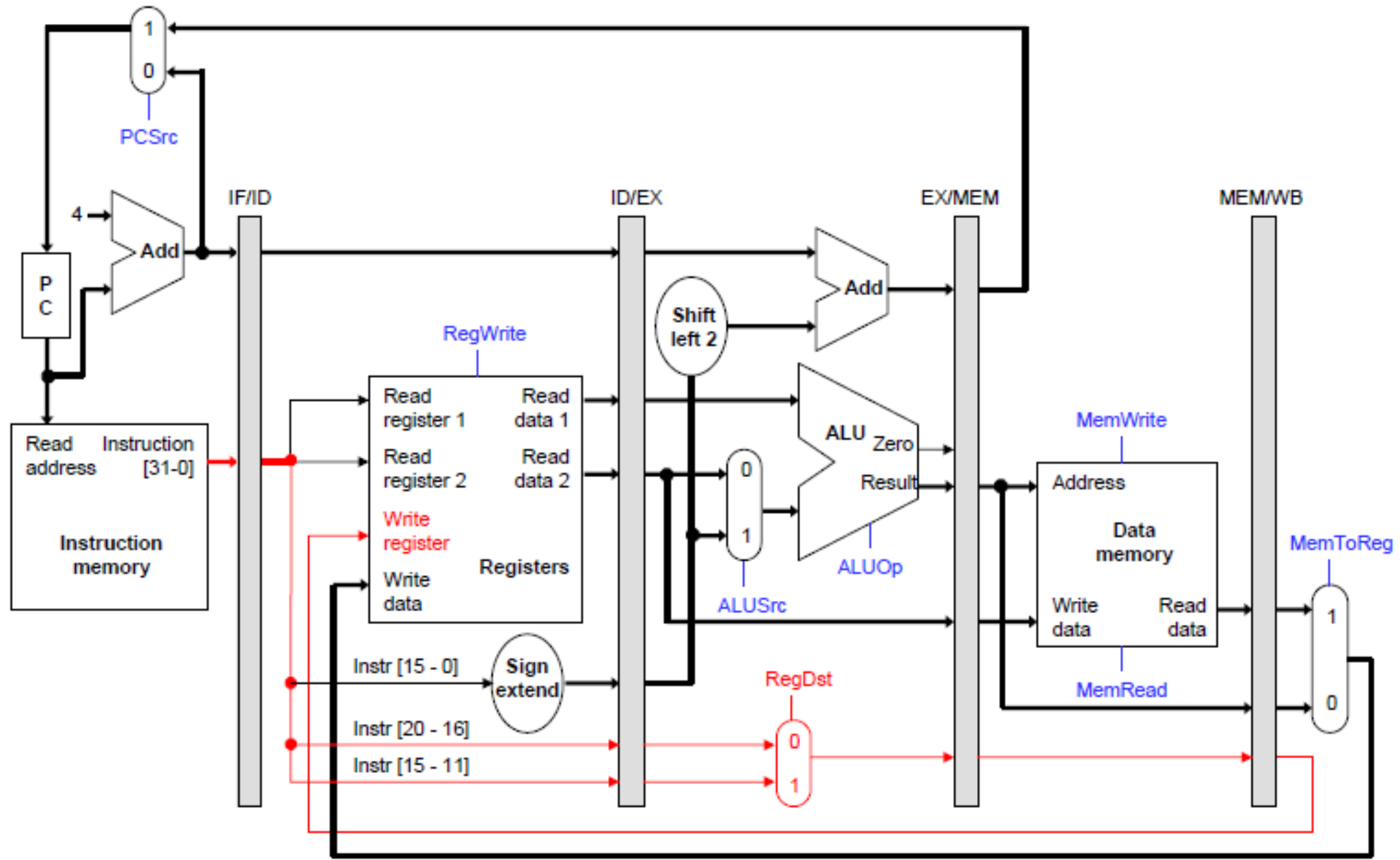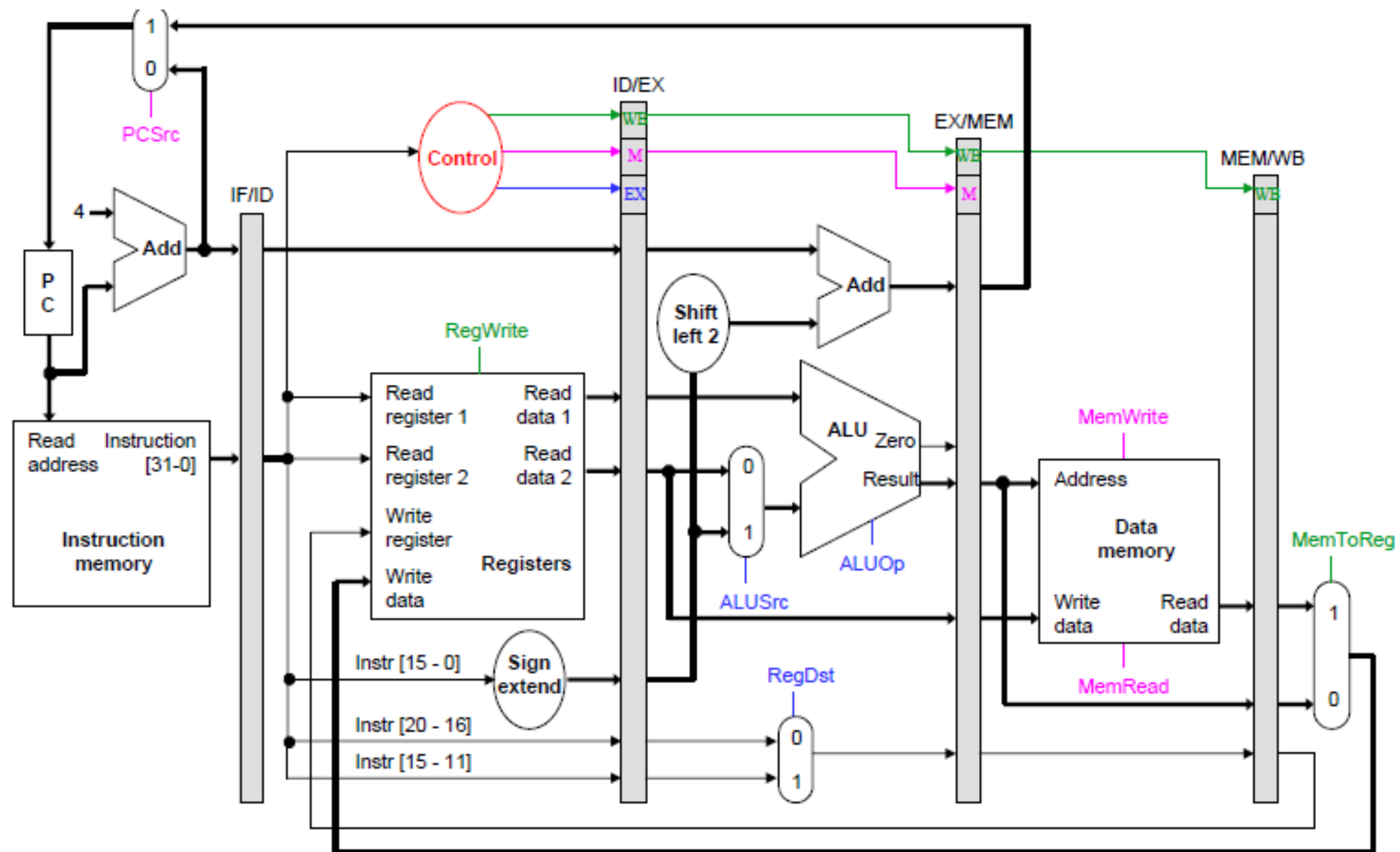# MIPS: Single-Cycle

Pipeline Datapath

Pipeline Datapath

Pipeline Controller

Stage	Control signals needed		
EX	ALUSrc	ALUOp	RegDst
MEM	MemRead	MemWrite	PCSrc
WB	RegWrite	MemToReg	

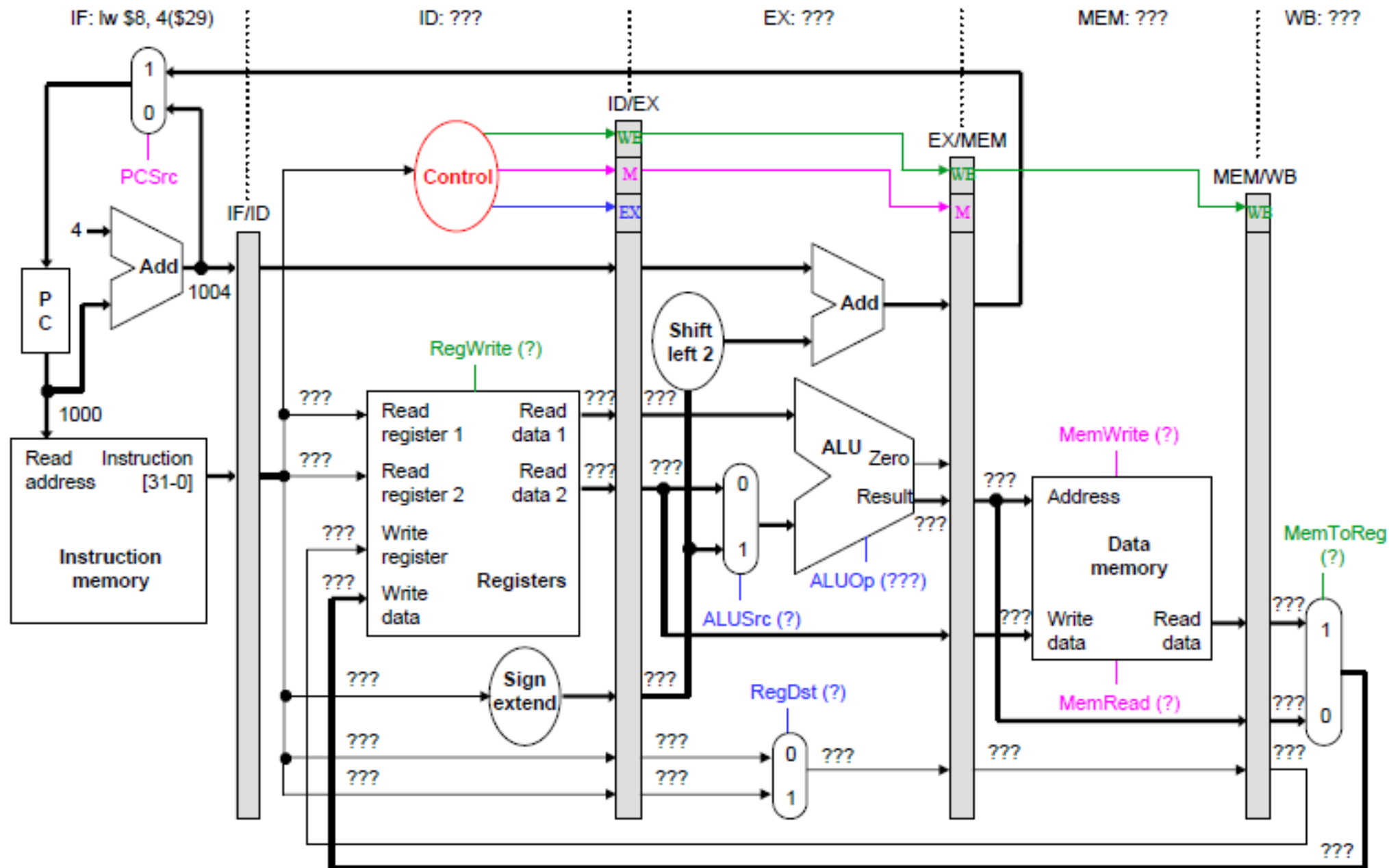# Pipeline Controller

How does pipeline work?

- ❖ **Assumption:**
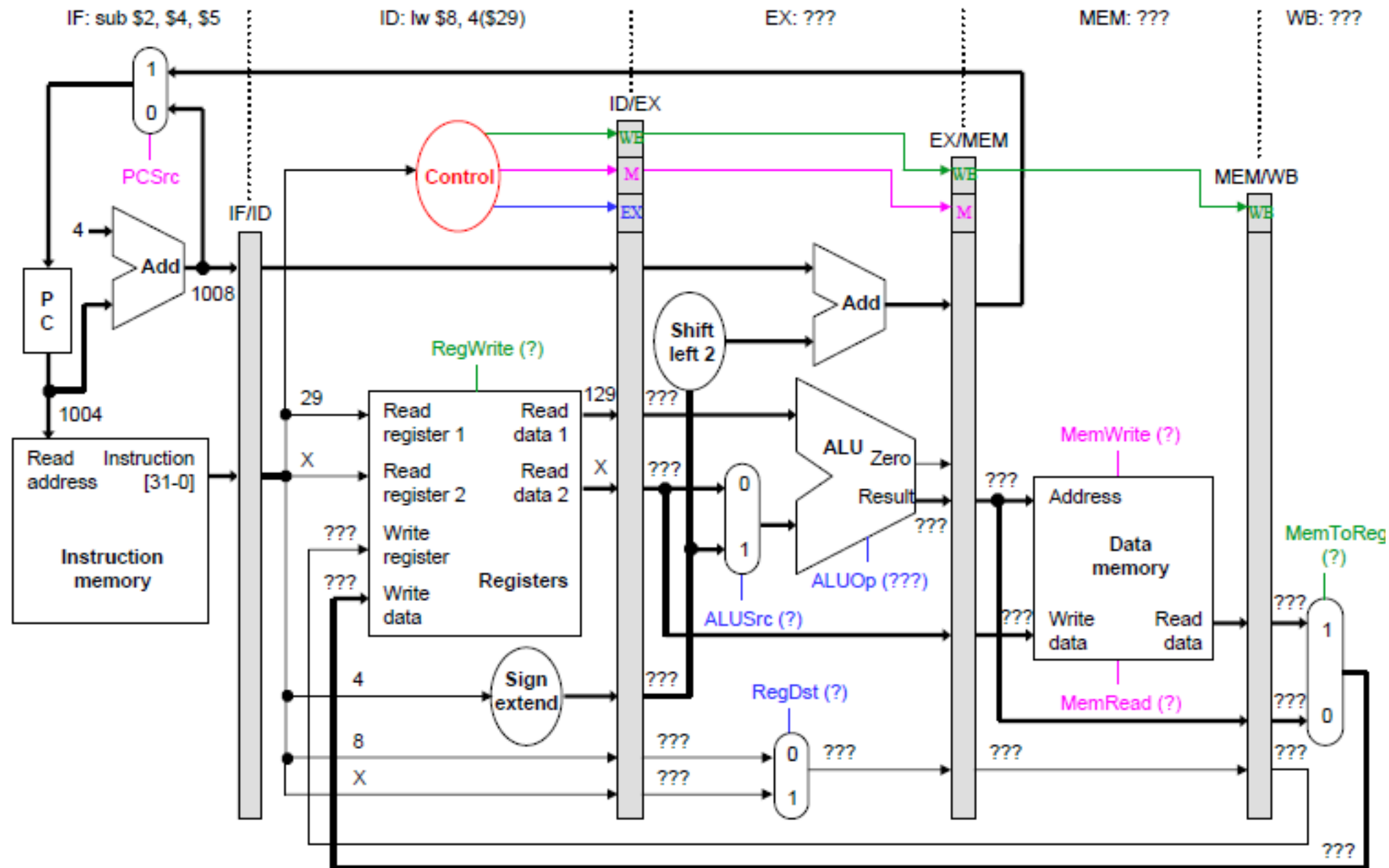   - ❖ **Ri ($i) = i + 100**
    - ❖ **Memory locations contain 99**

```
1000:  lw   $8, 4($29)
1004:  sub  $2, $4, $5
1008:  and  $9, $10, $11
1012:  or   $16, $17, $18
1016:  add  $13, $14, $0
```
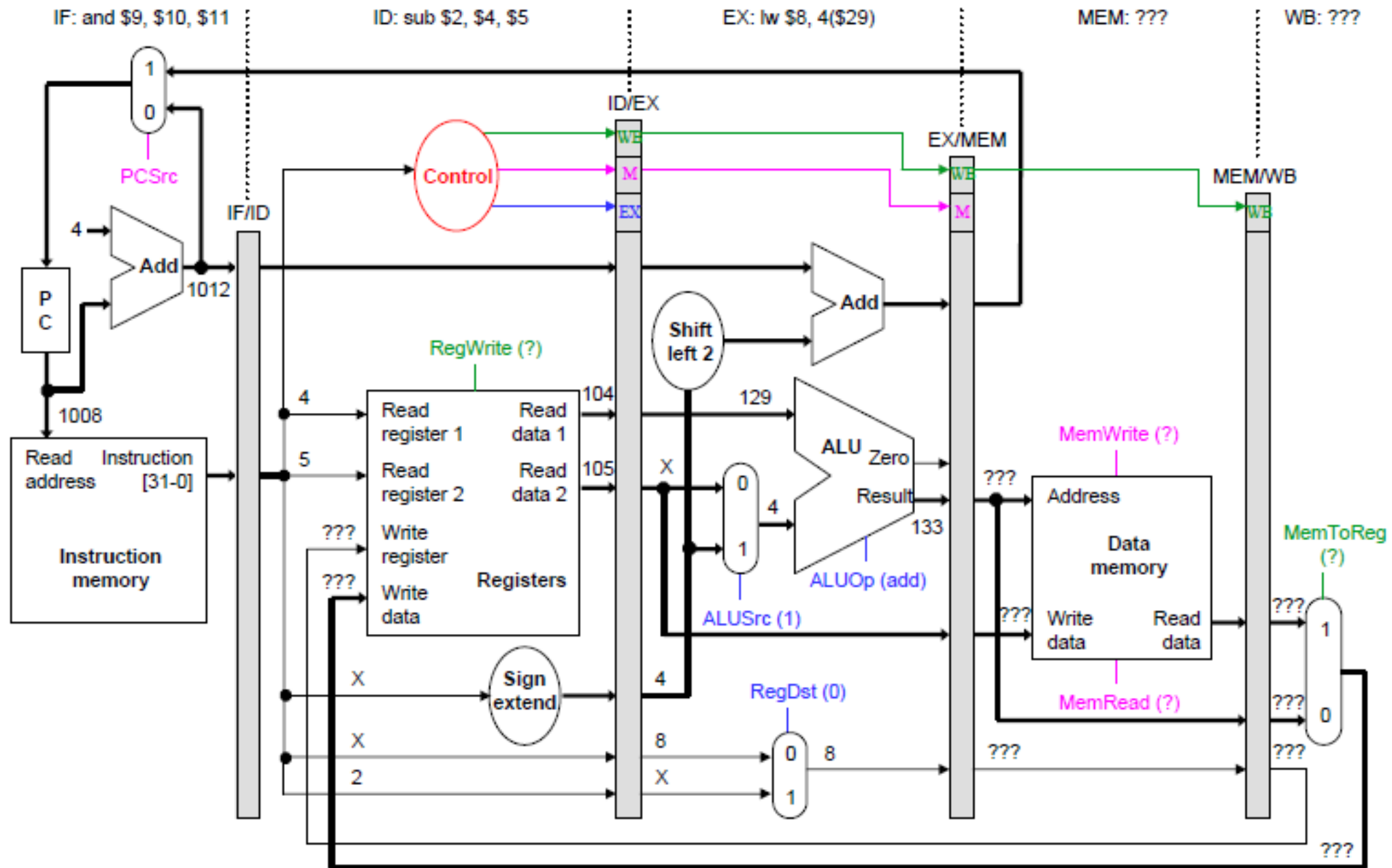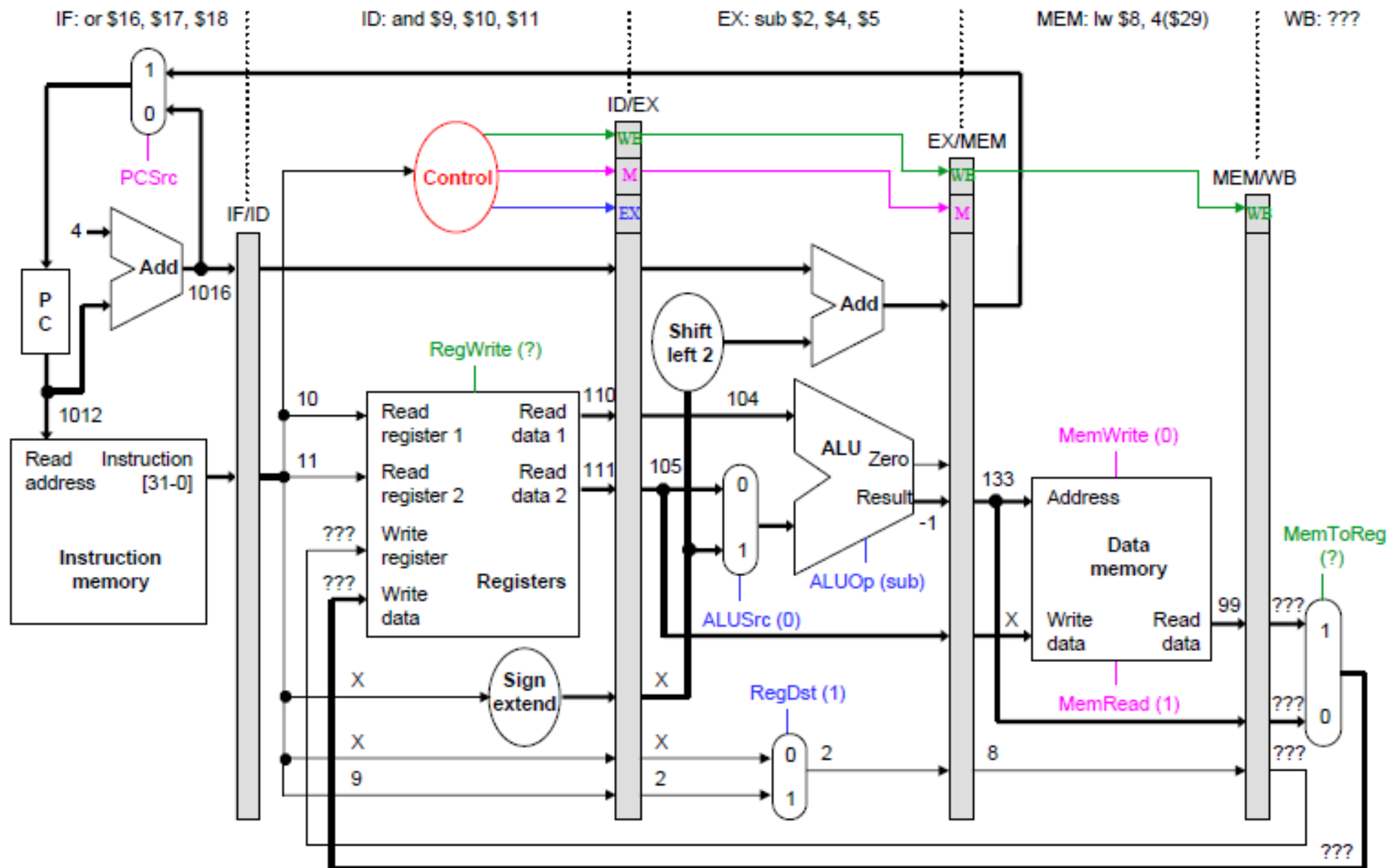
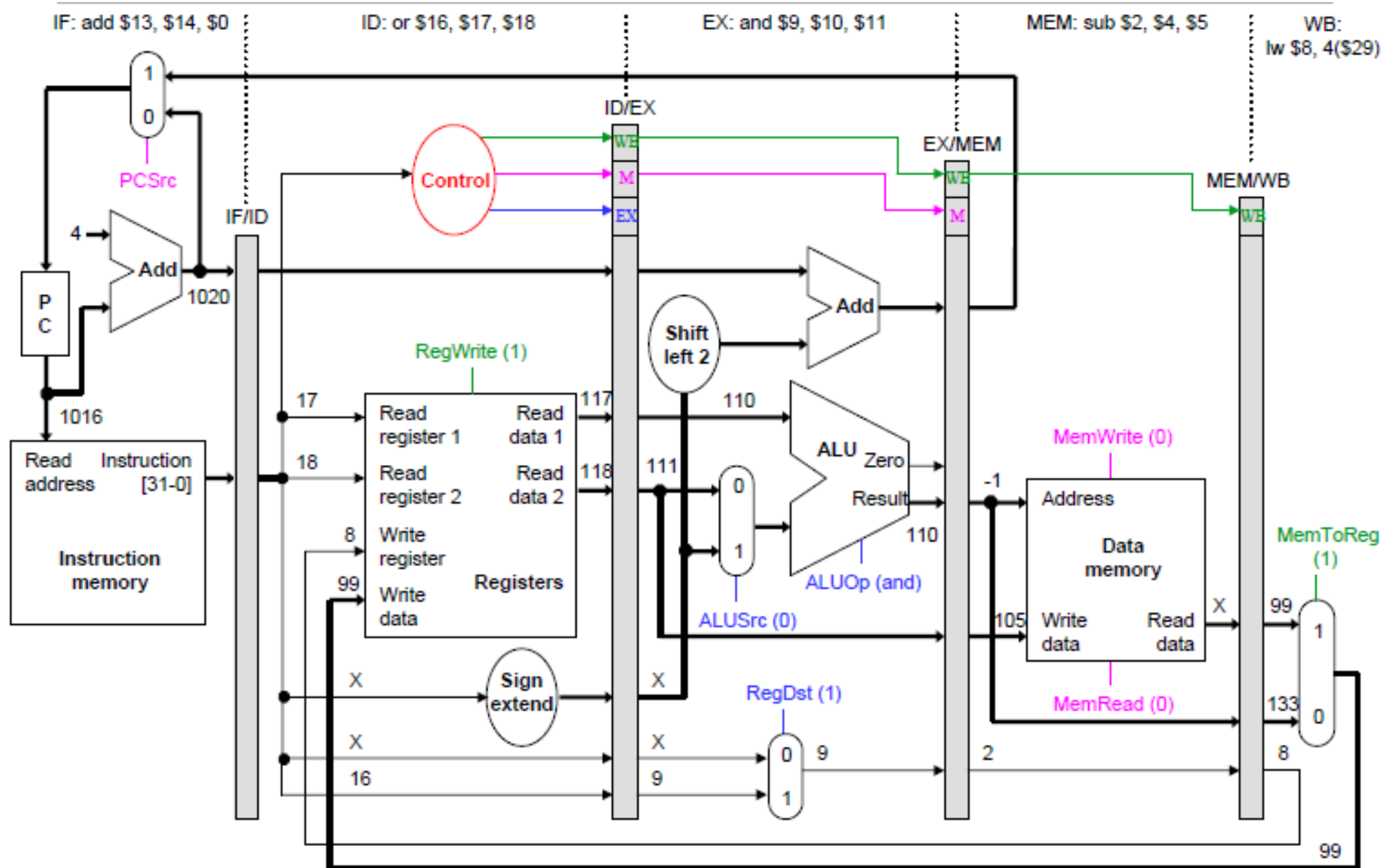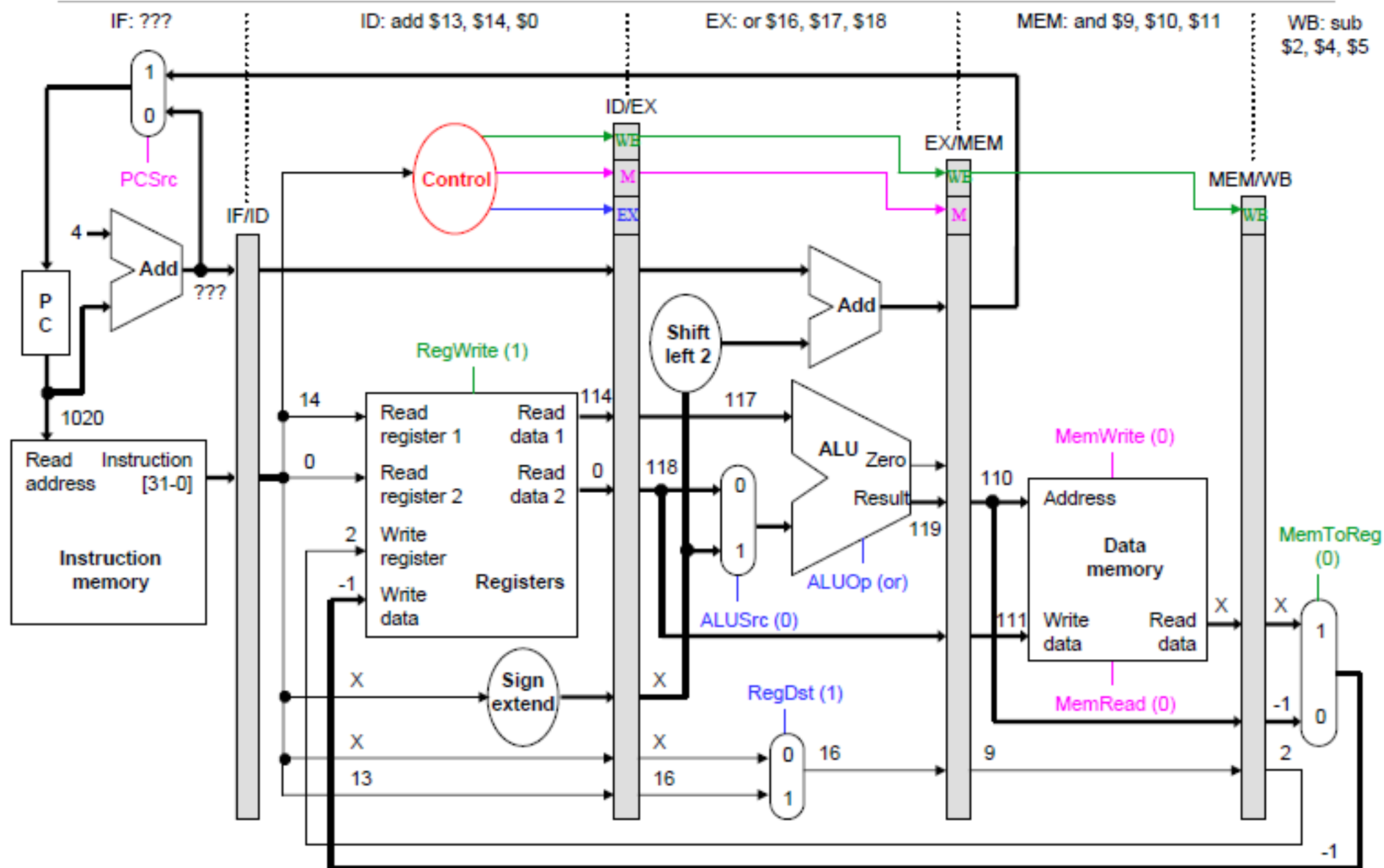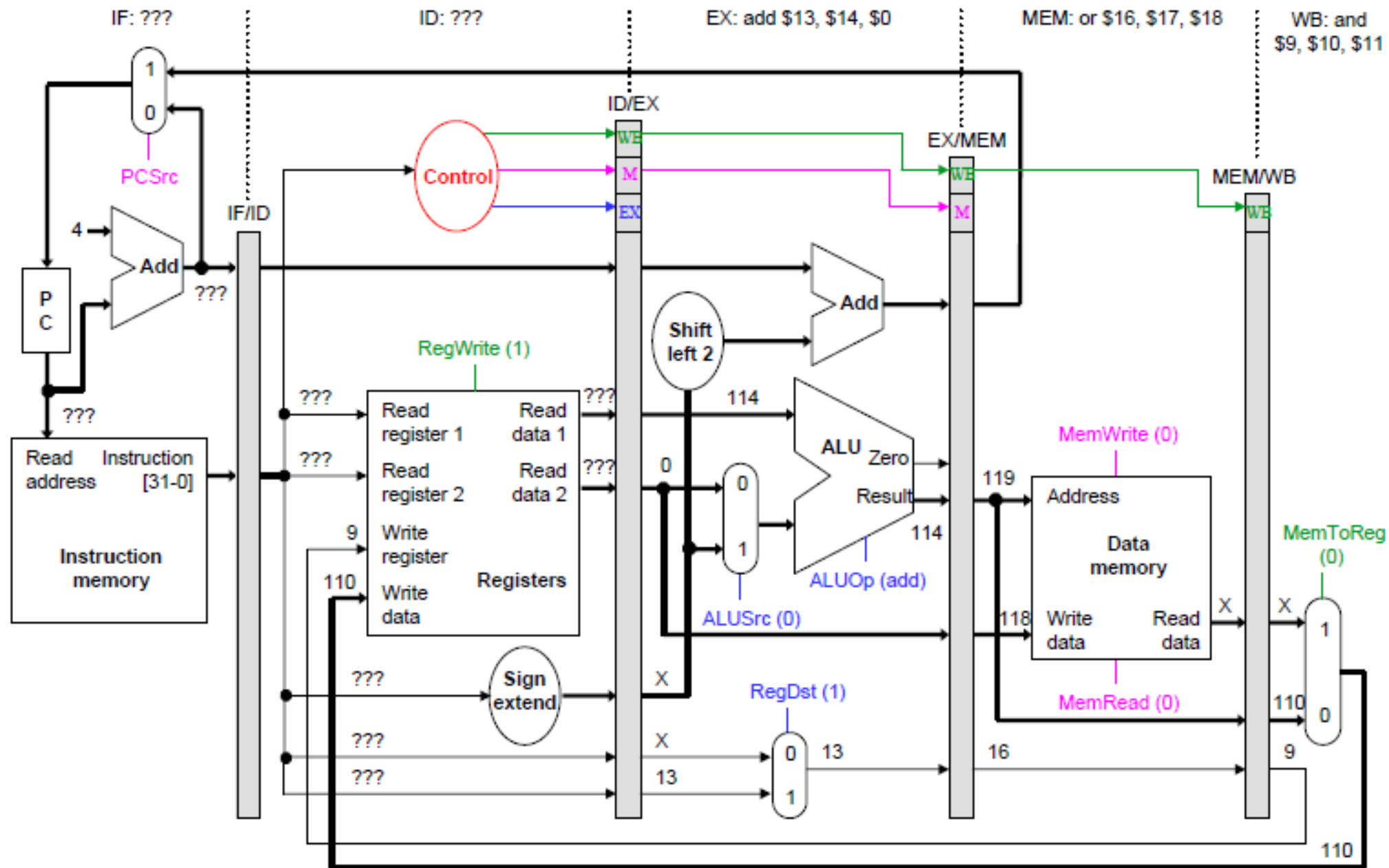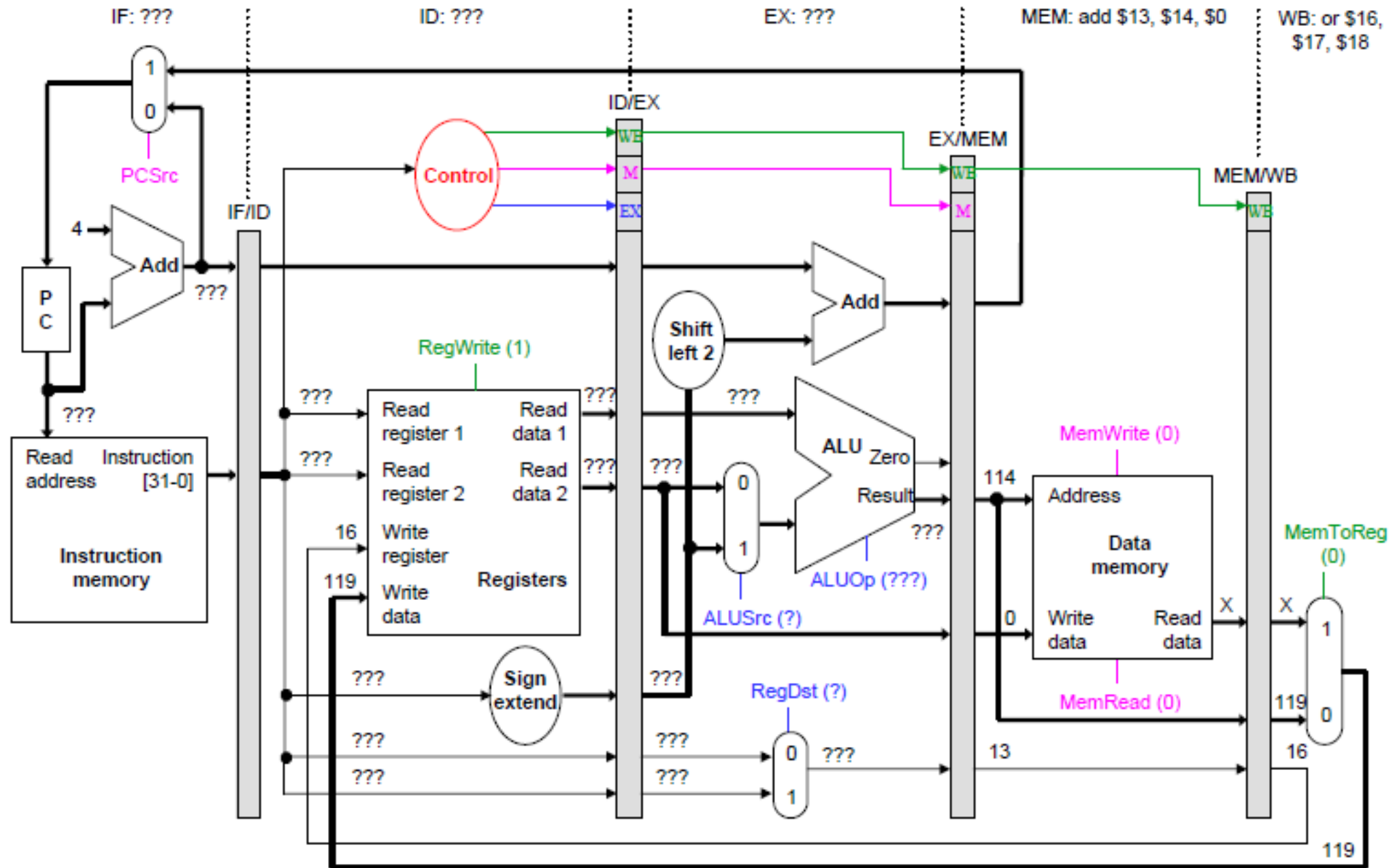# How does pipeline work?

How does pipeline work?

How does pipeline work?

How does pipeline work?

How does pipeline work?
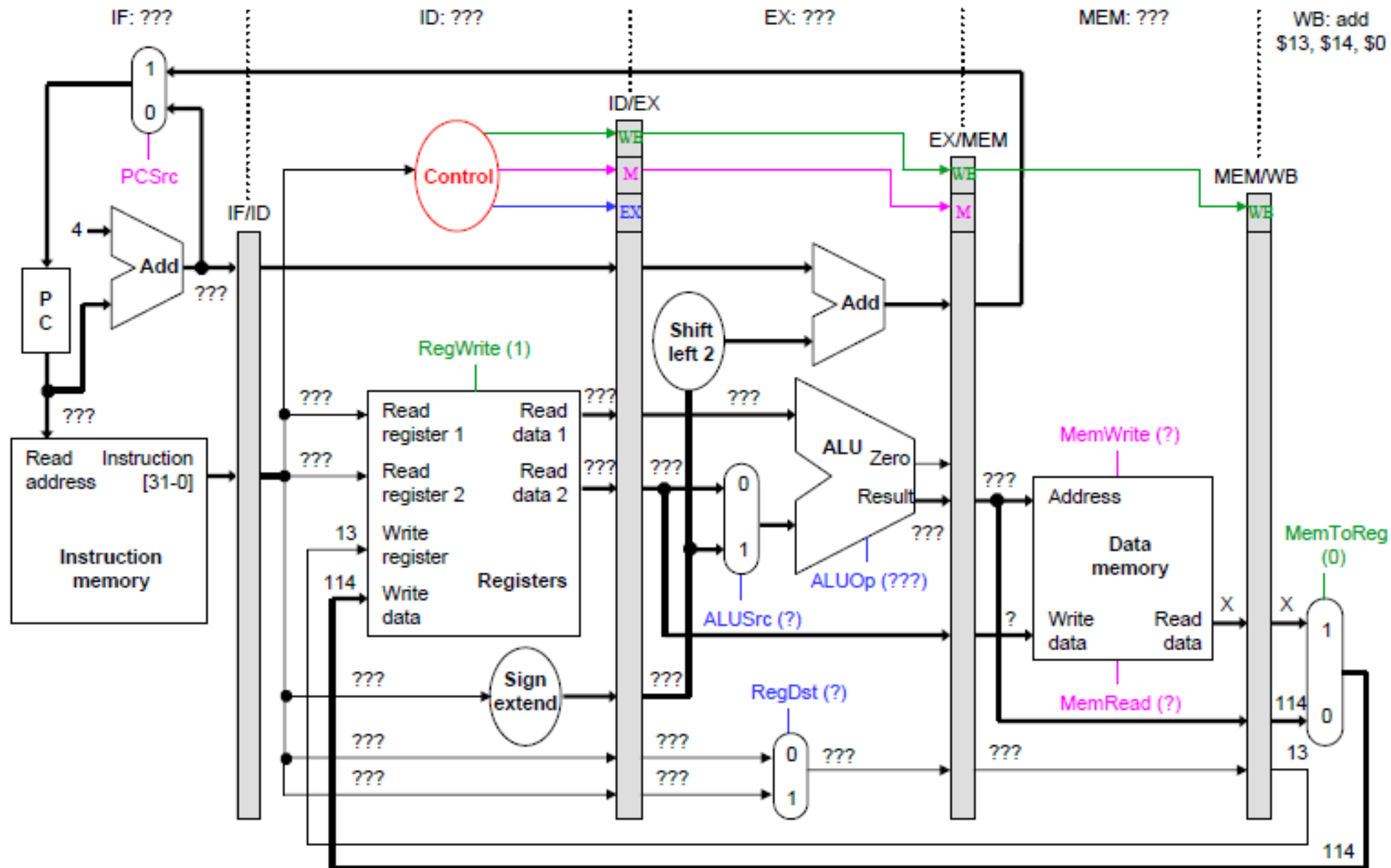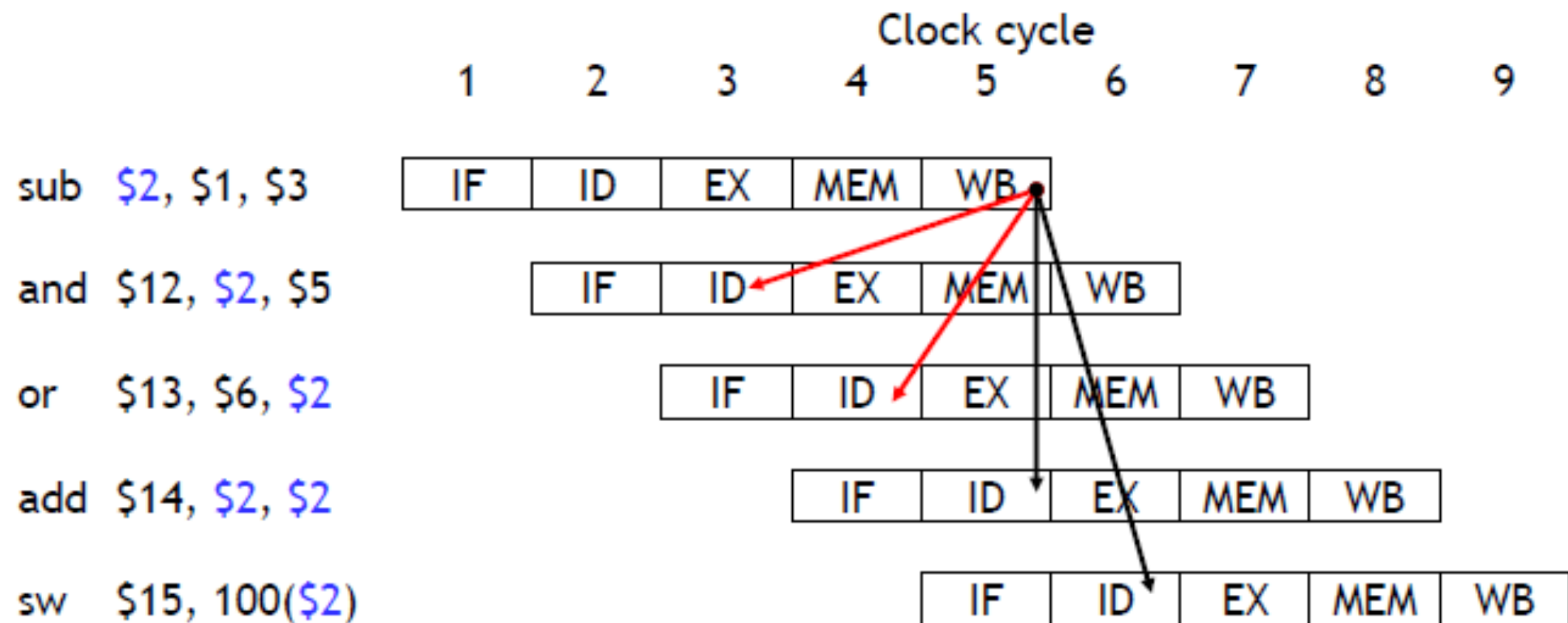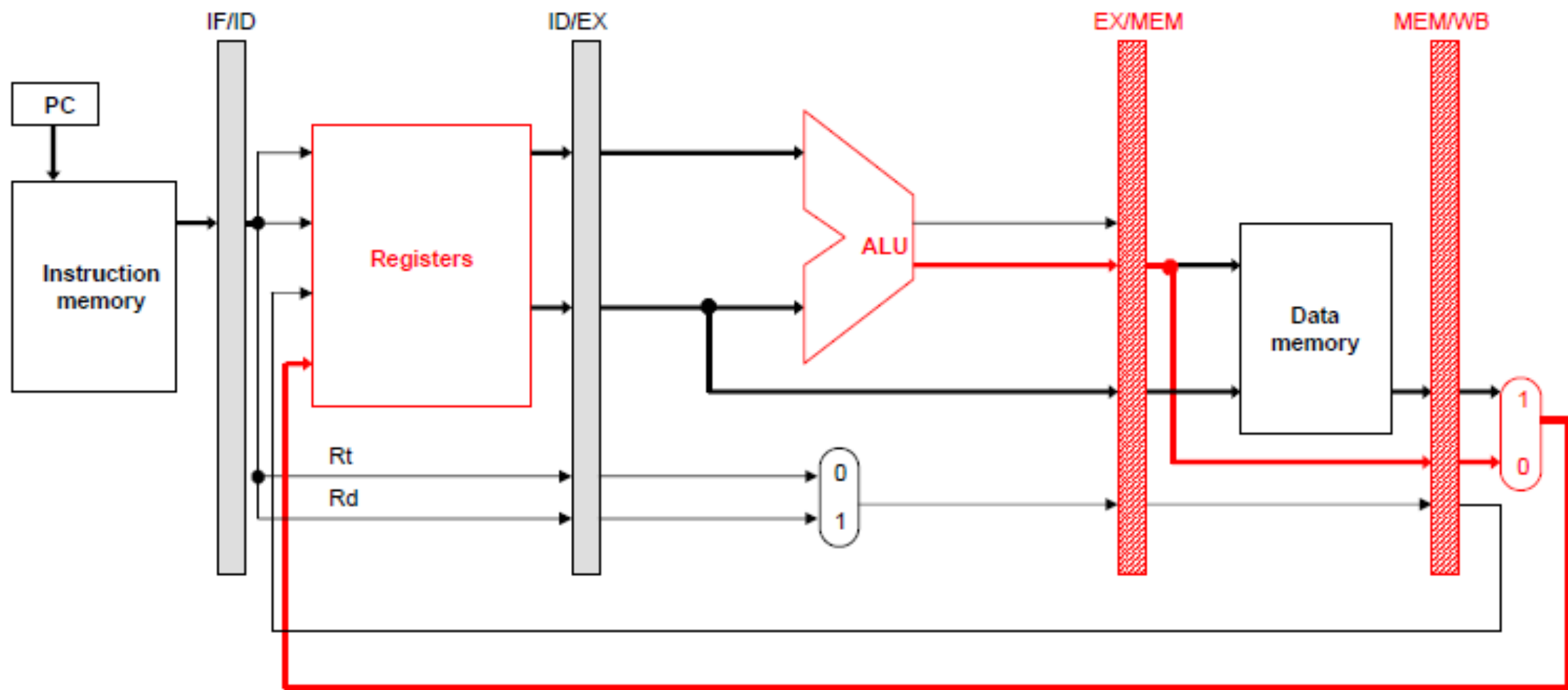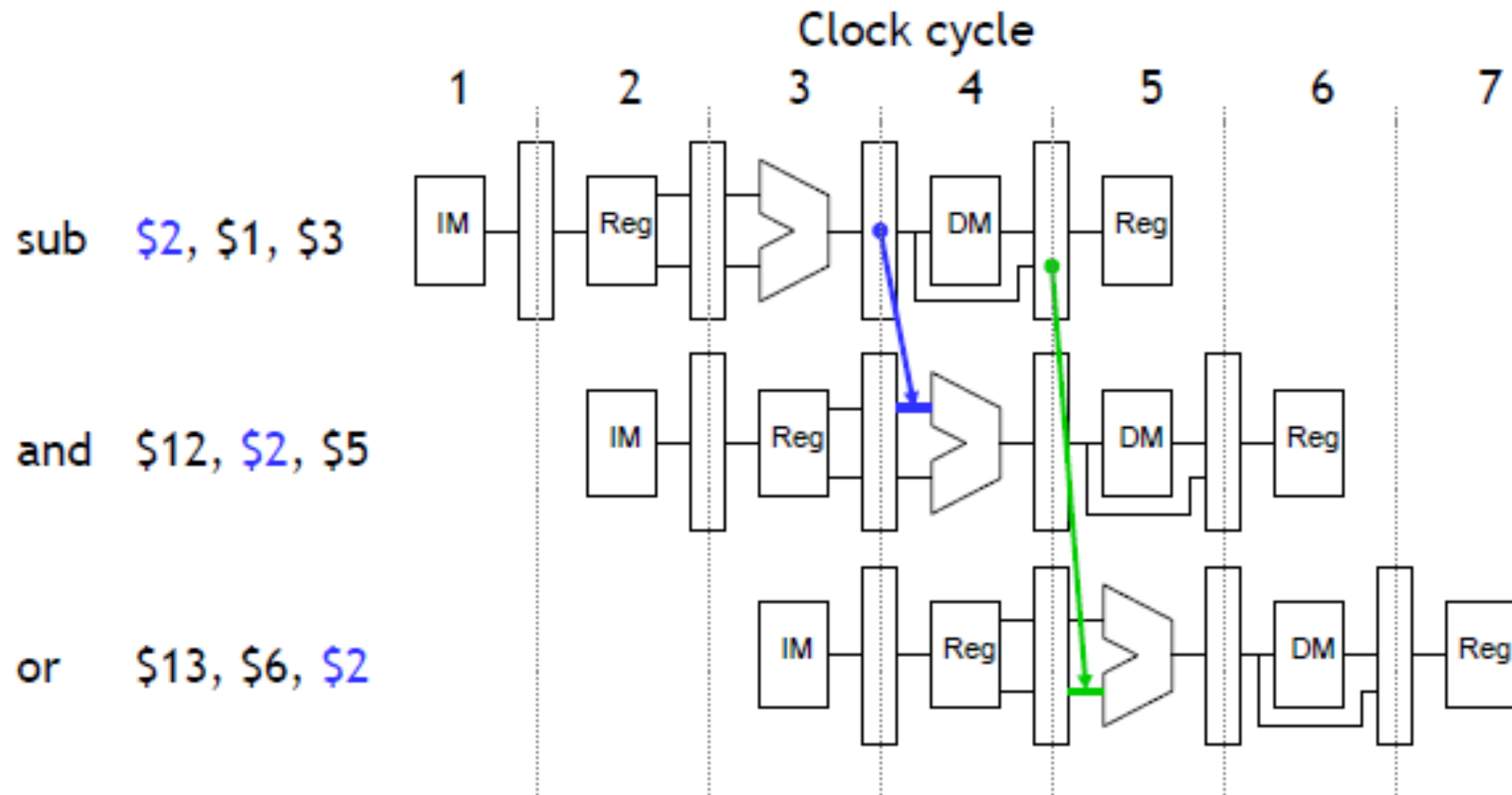
How does pipeline work?

How does pipeline work?

How does pipeline work?
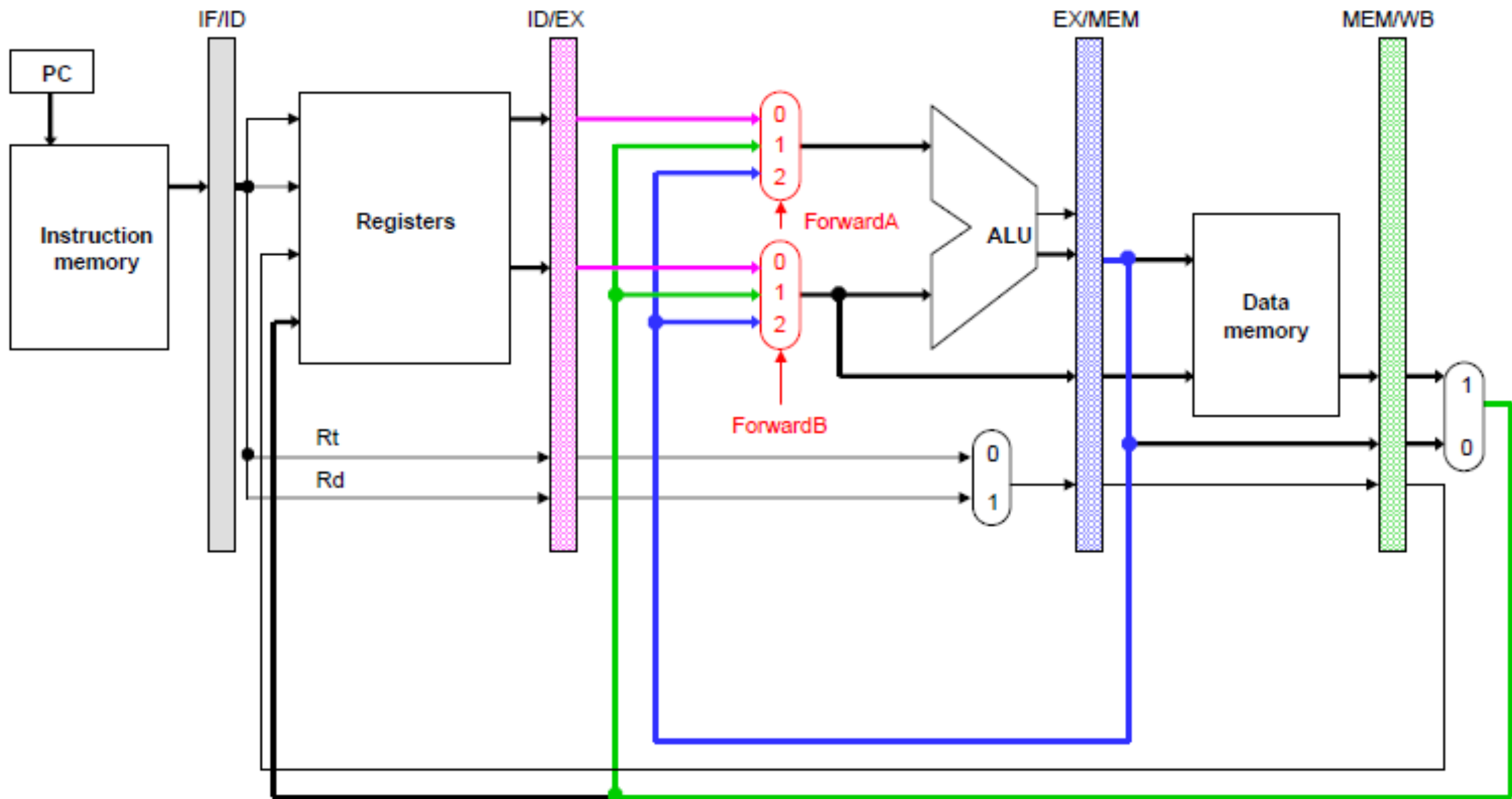
How does pipeline work?

Data Hazard

Data Hazard

Saeed Safari
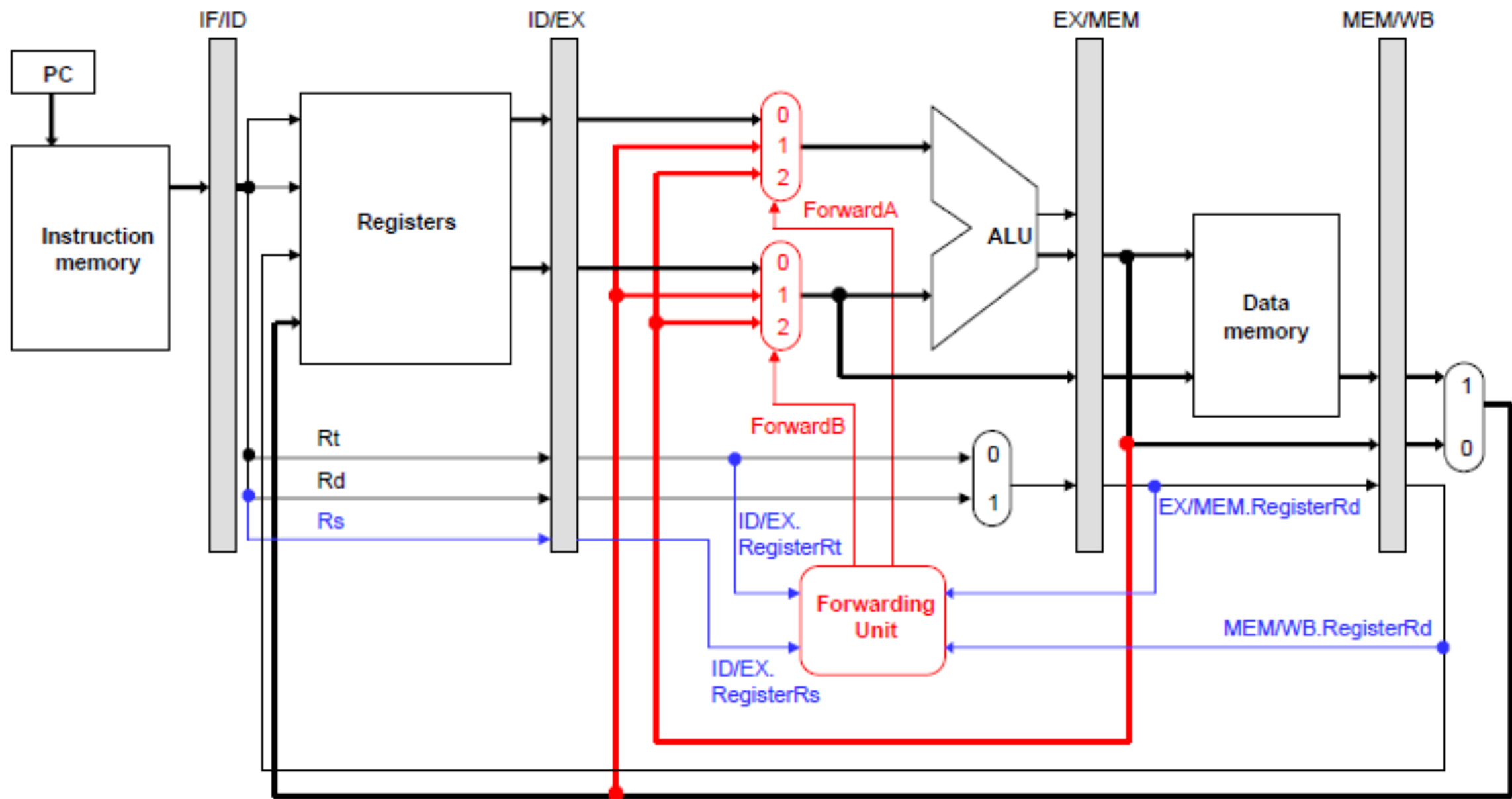ECE School, Faculty of Engineering,
University of Tehran

Data Hazard

Data Forwarding

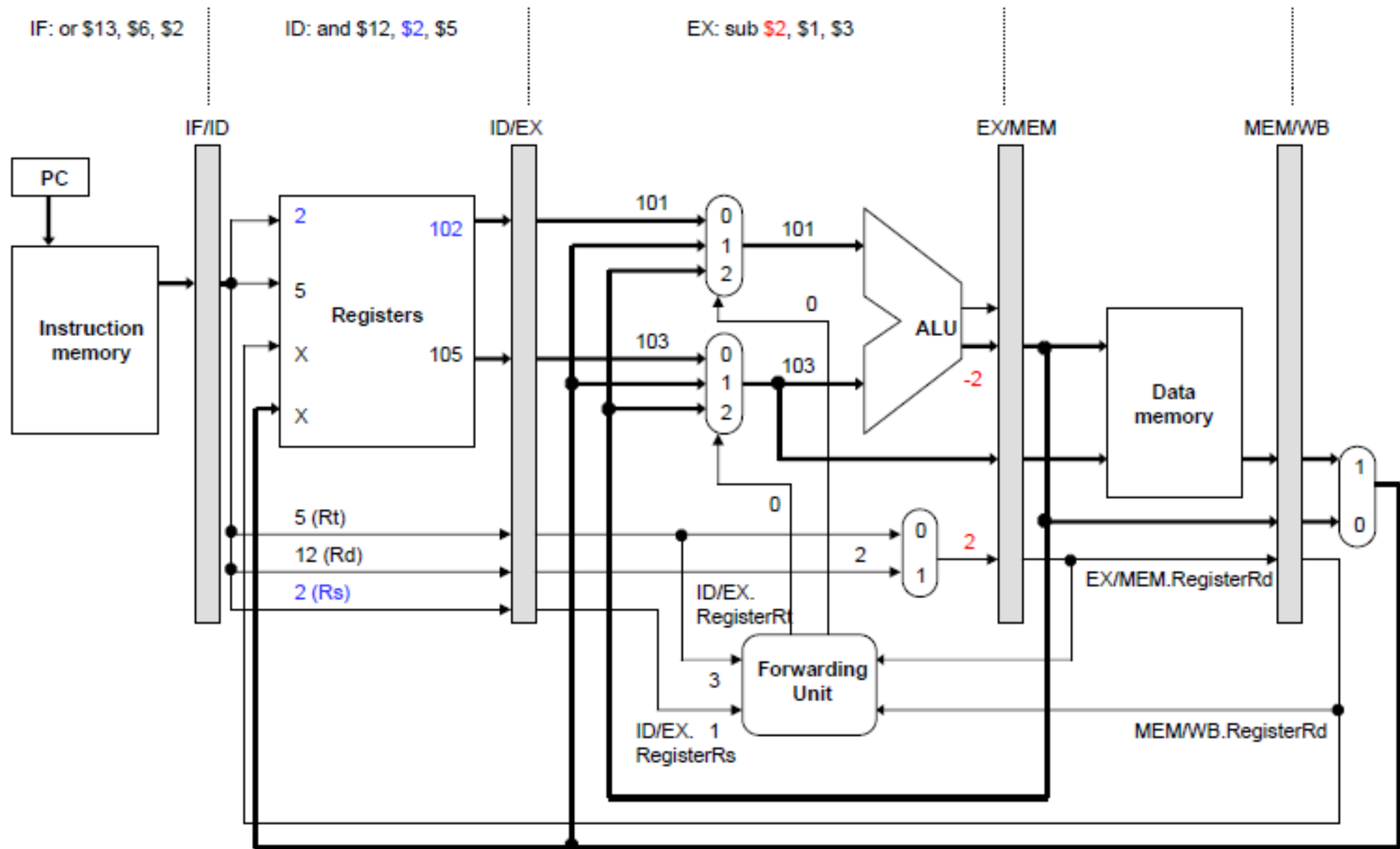# Forwarding Unit

How does FW unit work?

How does pipeline work?

```
sub    $2, $1, $3
and    $12, $2, $5
or     $13, $6, $2
add    $14, $2, $2
sw     $15, 100($2)
```
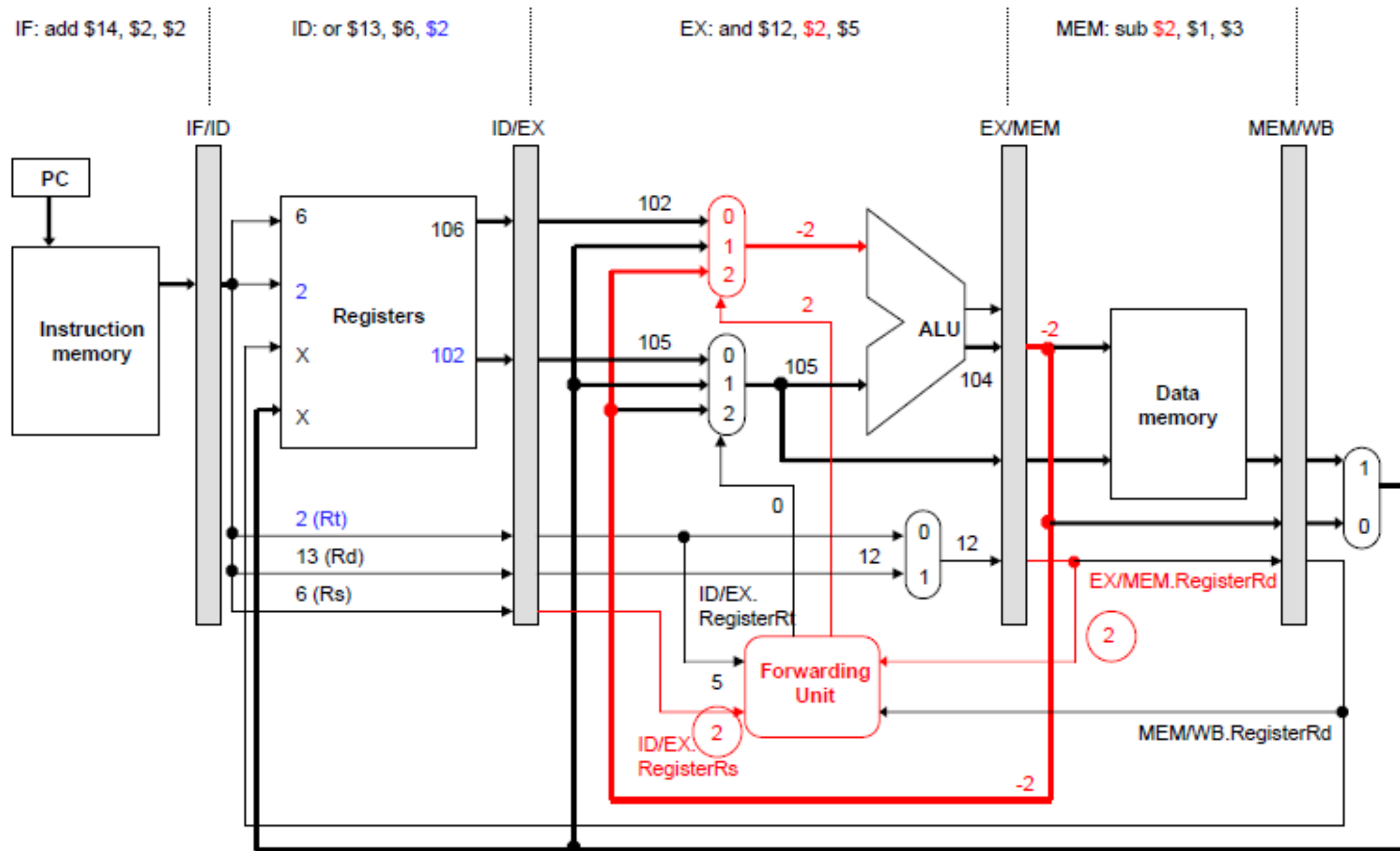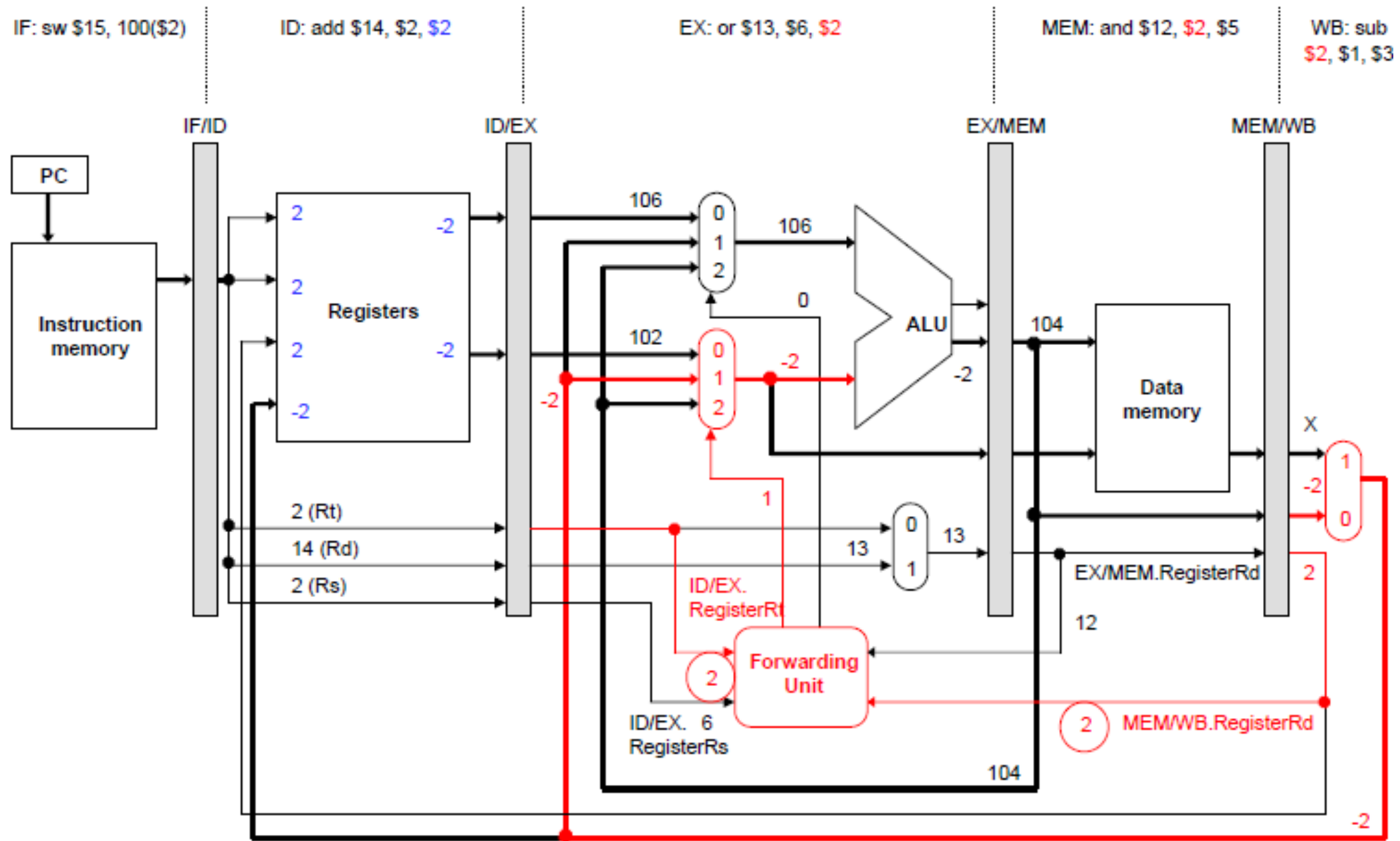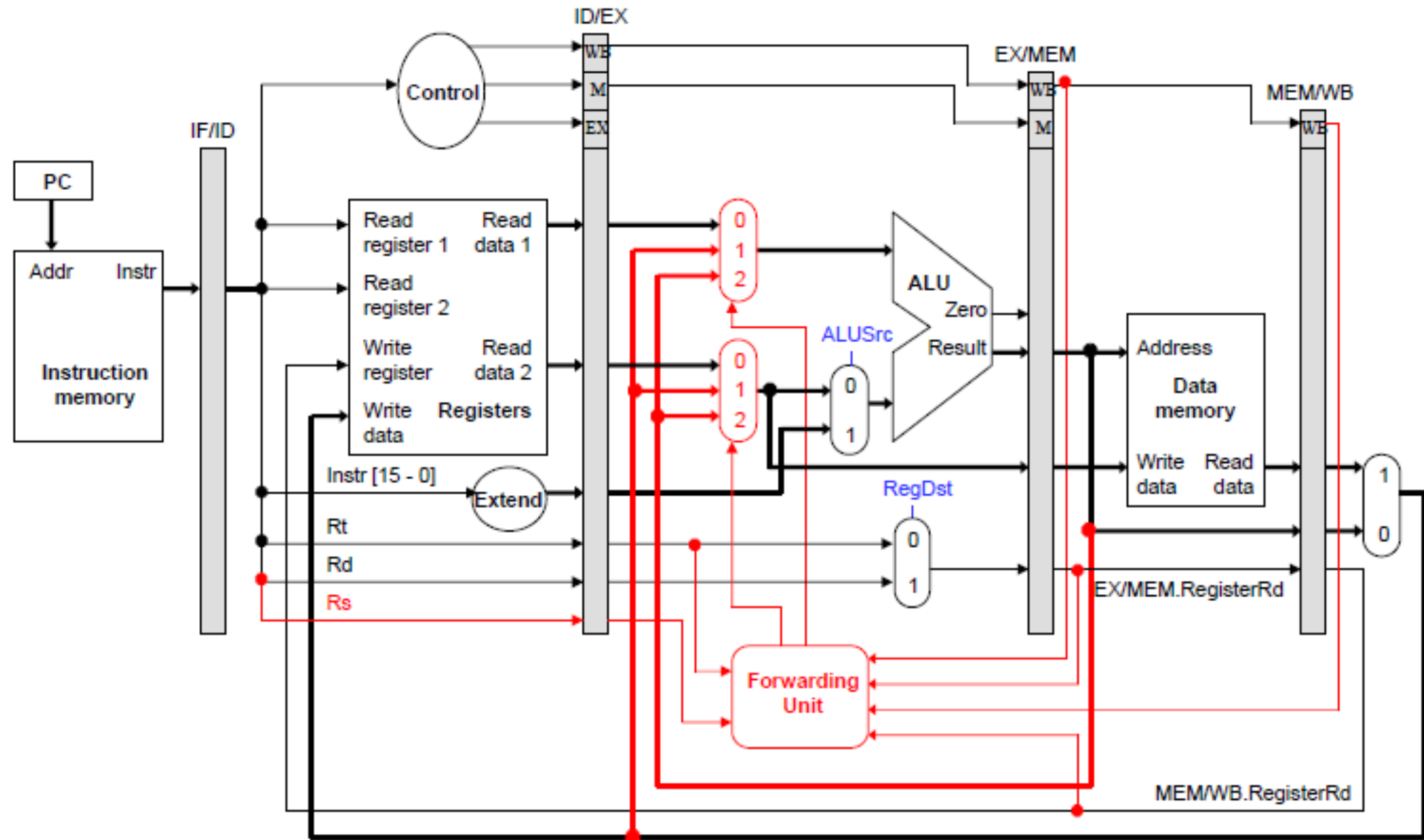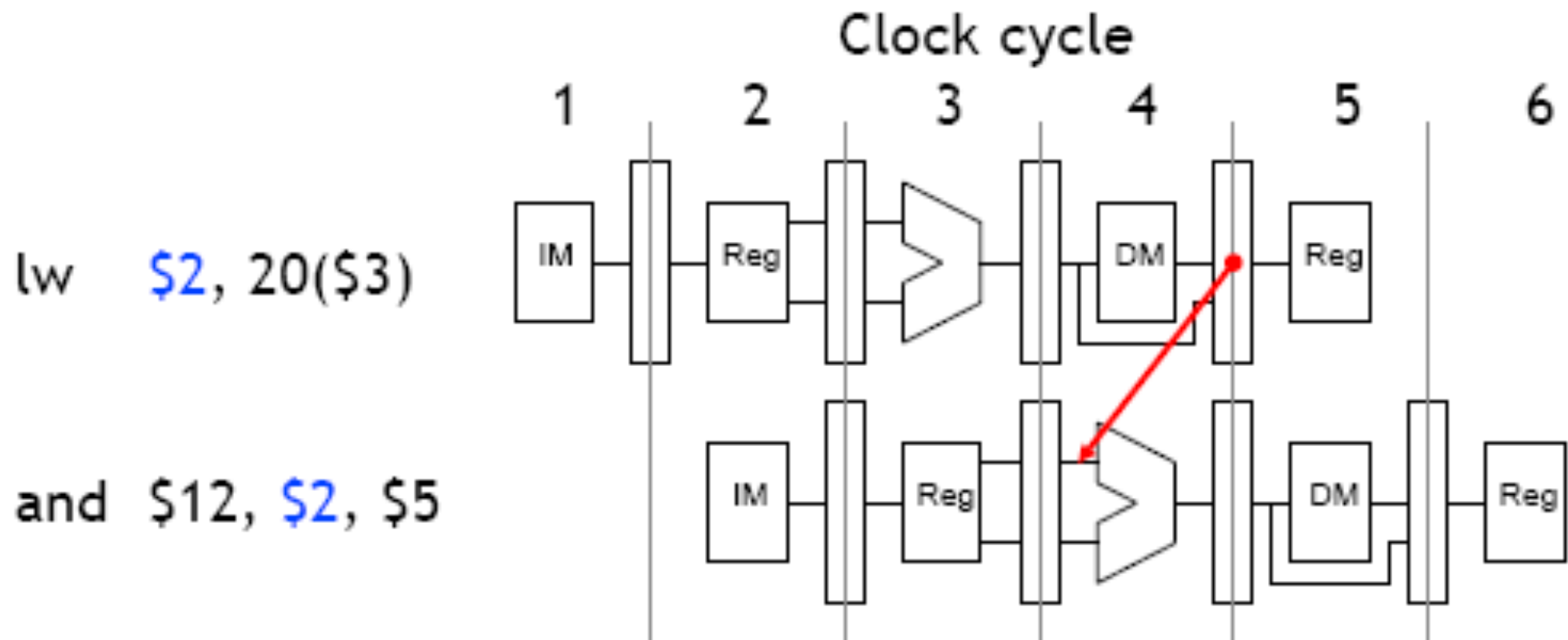
How does pipeline work?

How does pipeline work?
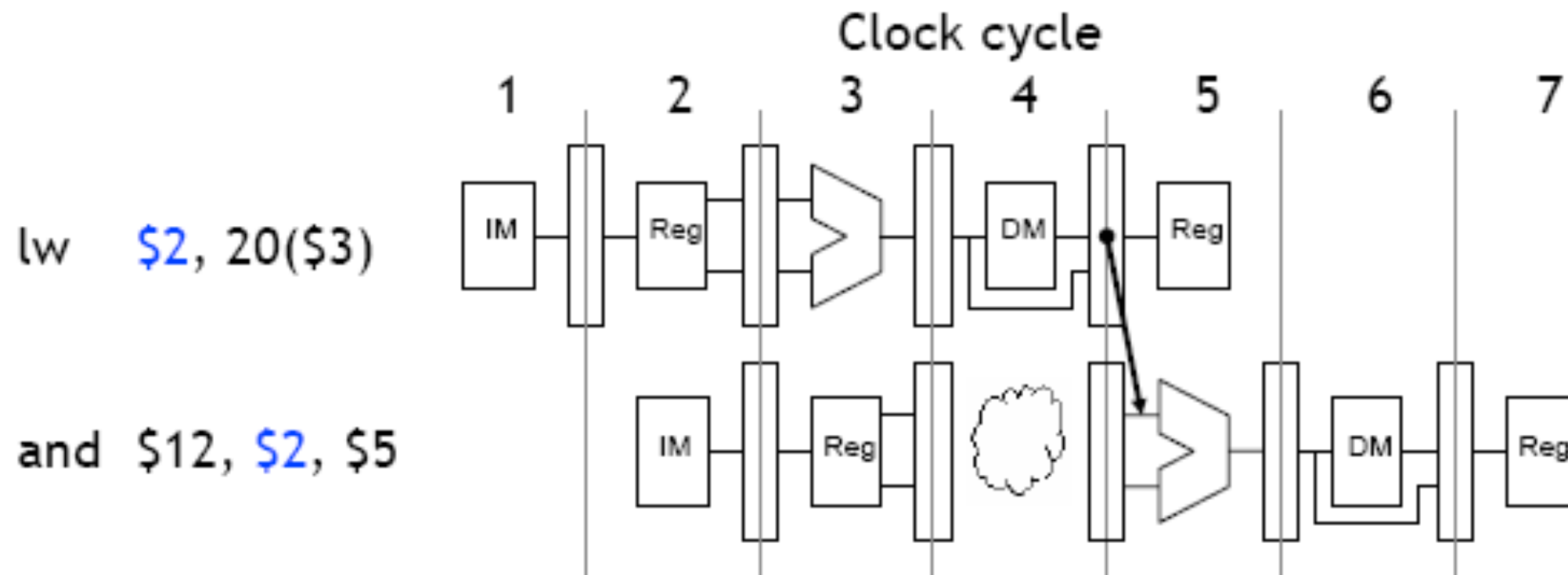
How does pipeline work?
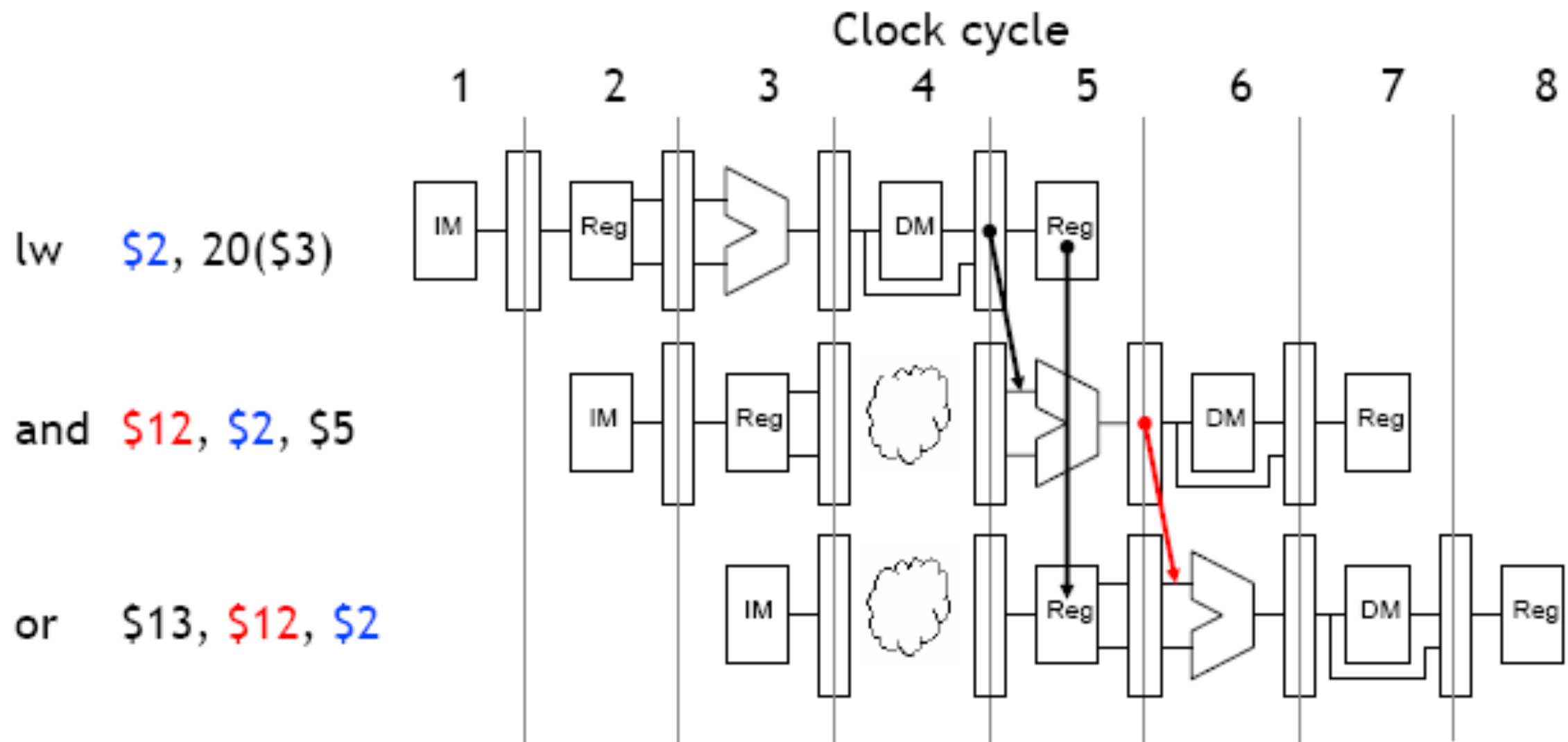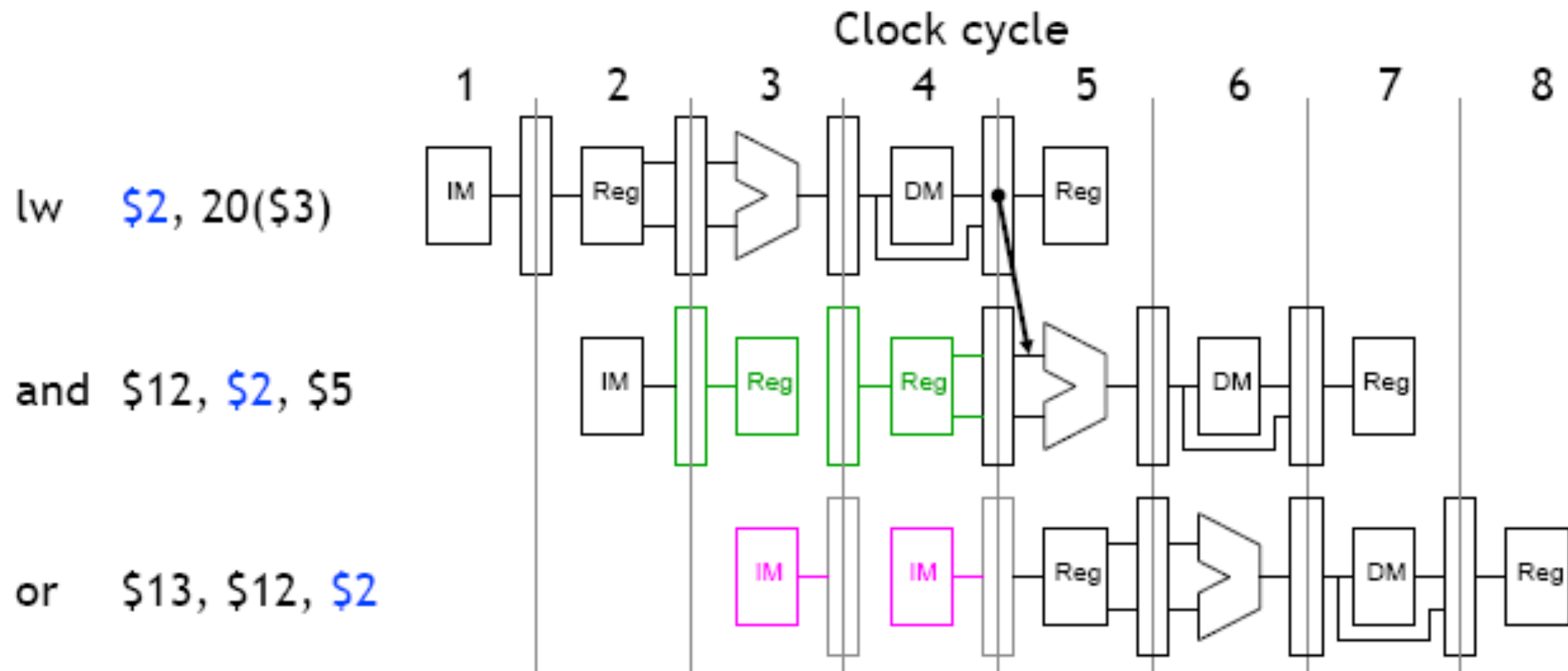
MIPS: Pipeline Implementation

Why do we need to stall pipeline?

Why do we need to stall pipeline?

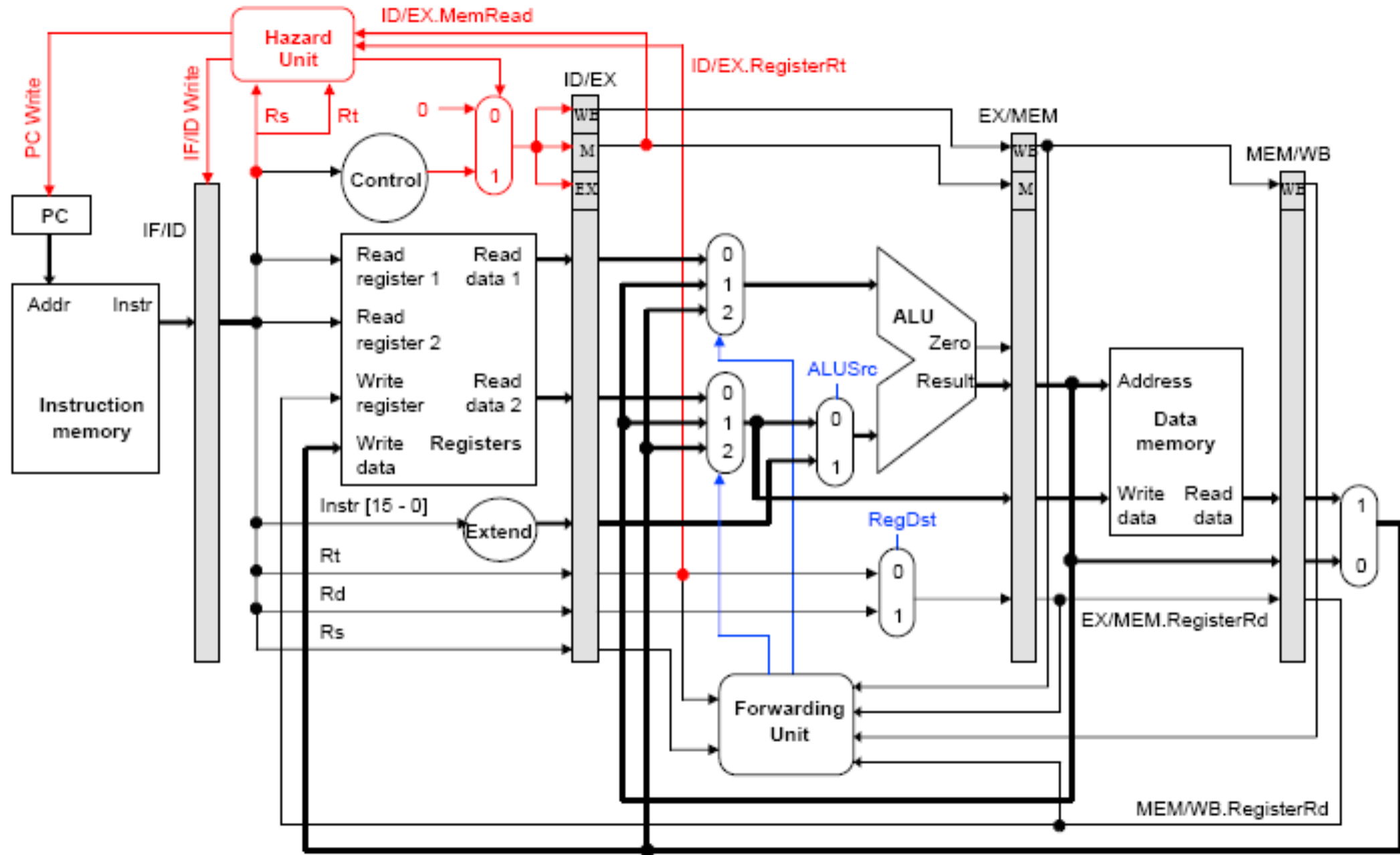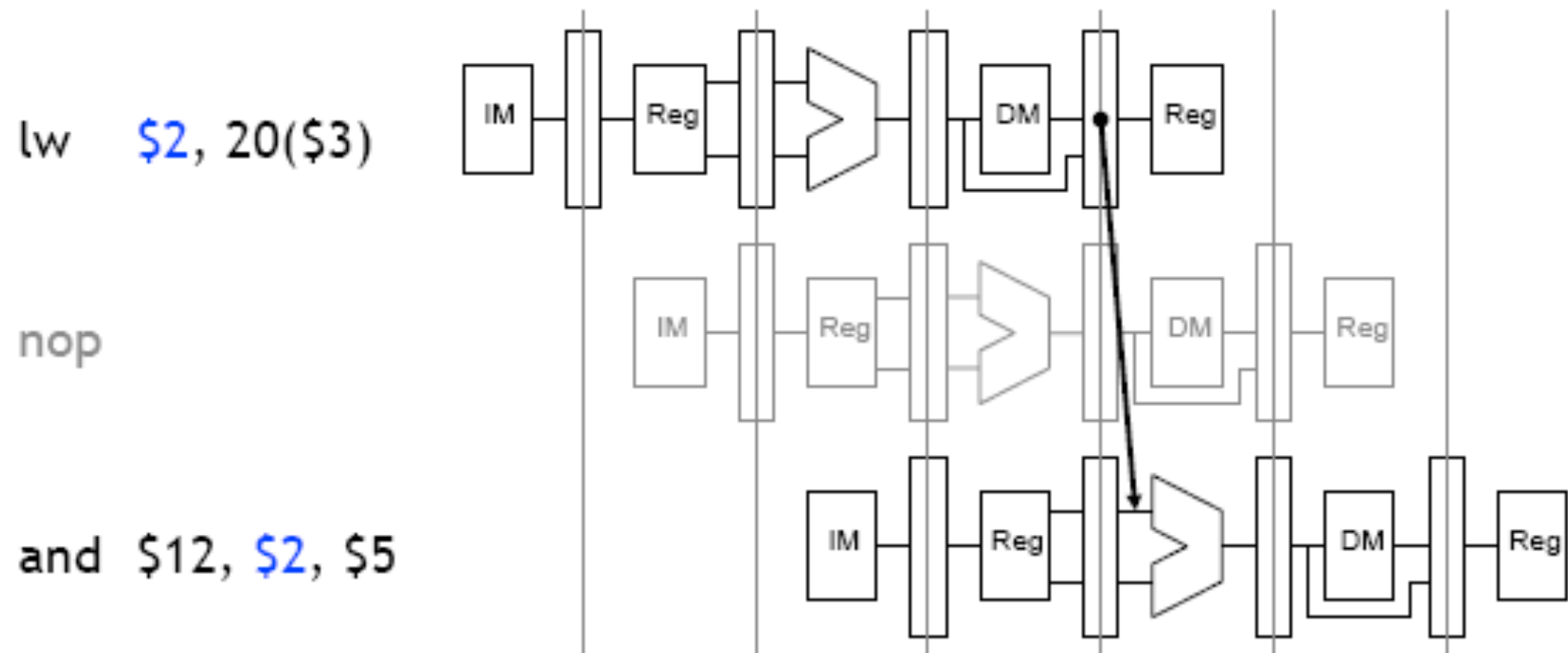# Why do we need to stall pipeline?

Why do we need to stall pipeline?

Pipeline with Stall

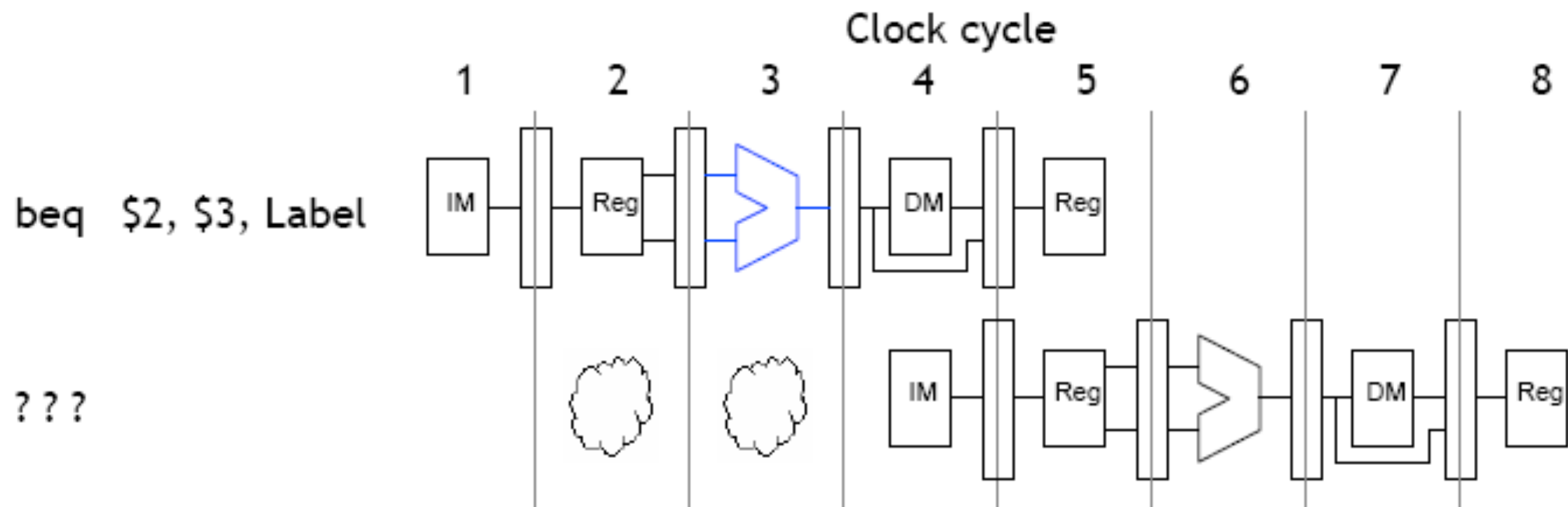# Pipeline with Stall

lw $2, 20($3)

nop

and $12, $2, $5

Control Hazard

Control Hazard

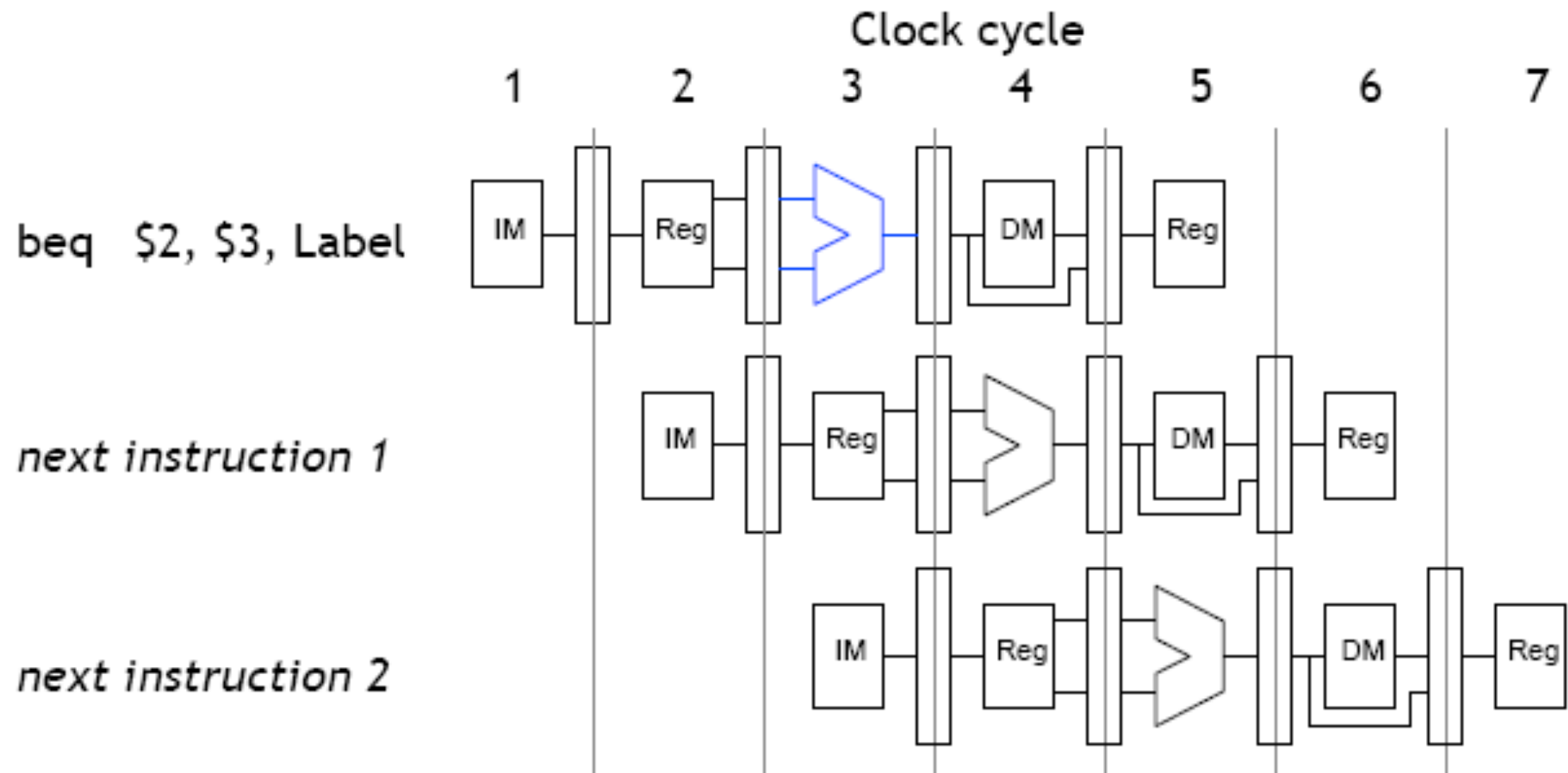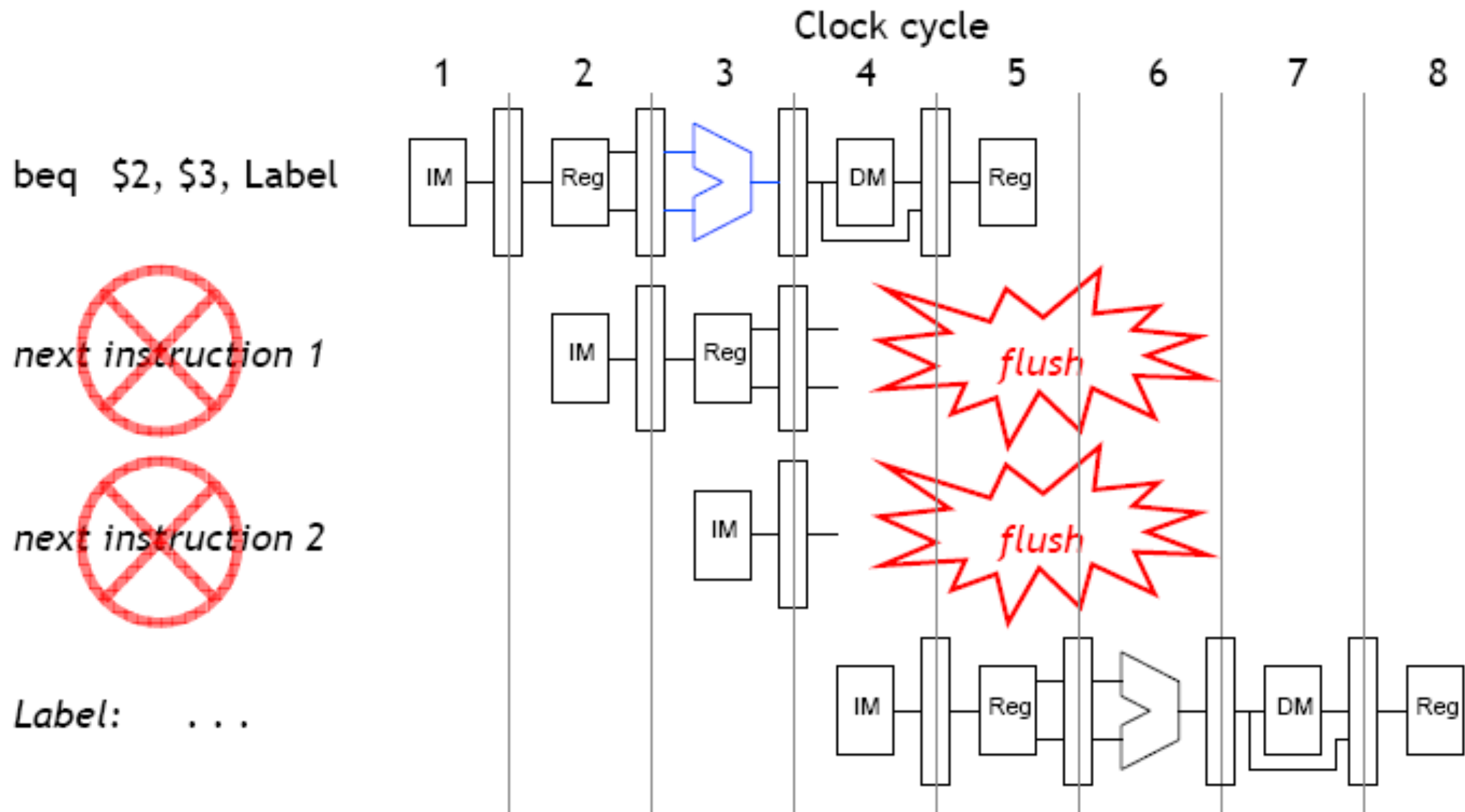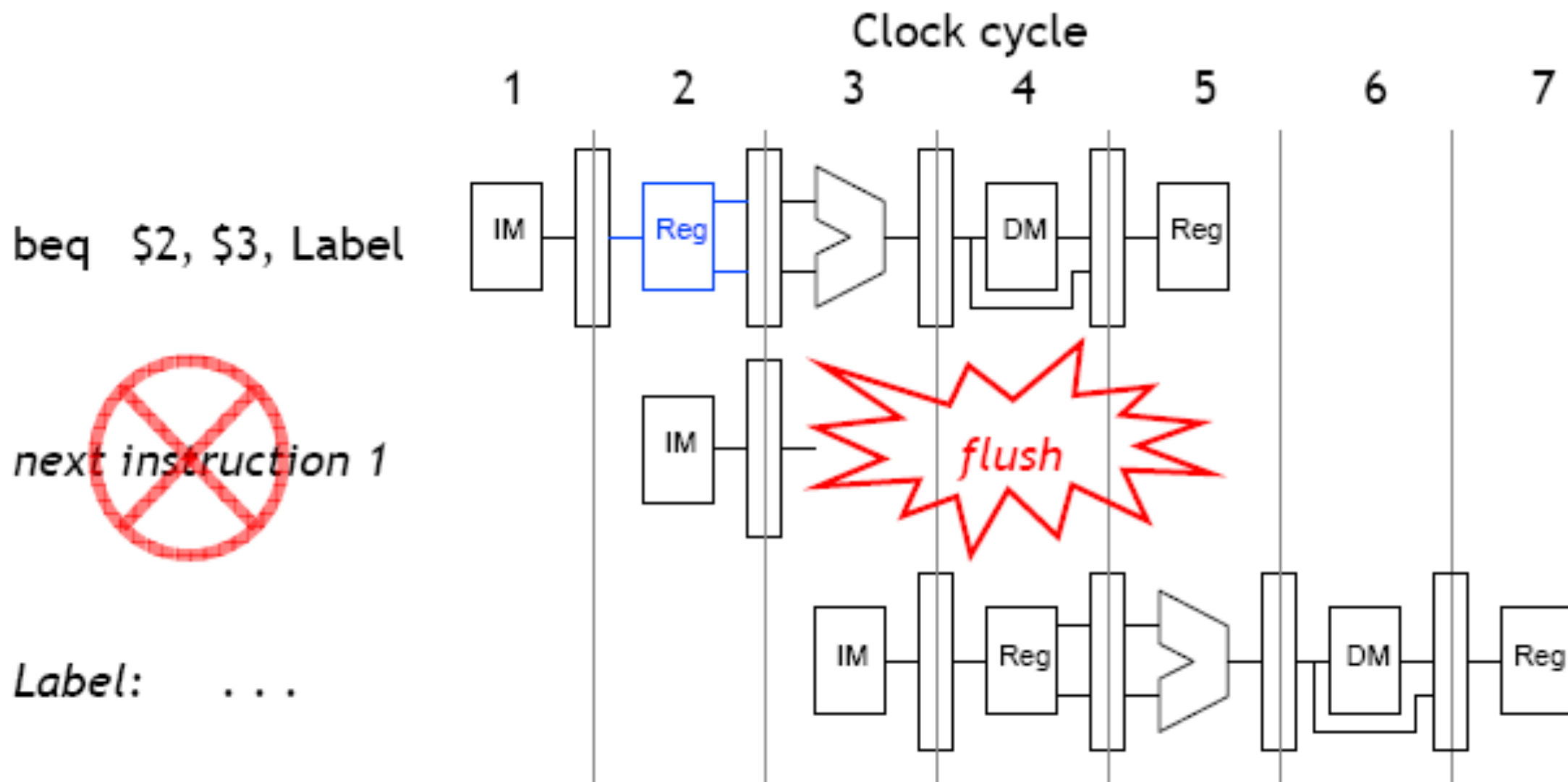# Branch Prediction

Branch Prediction

Branch Prediction

Branch Prediction