UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital System Design with Hardware Description Languages
Fall 1393 / Test 1

Computer Account#_____

First Name:_____

Last Name:_____

Number:_____

Signature:_____

Grade:

Problem 1. _____/

Problem 2. _____/

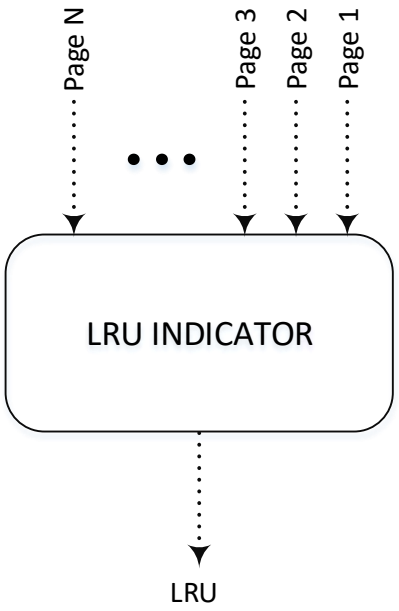
Problem 3. _____/

Problem 4. _____/

Total: _____/ 100

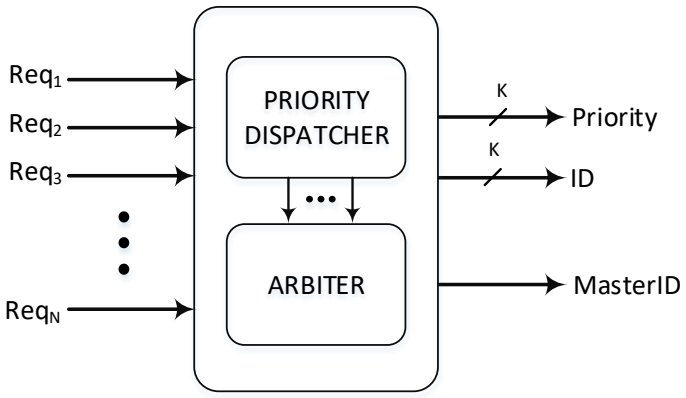
THIS IS AN OPEN BOOK OPEN NOTE EXAM
YOU HAVE EXACTLY TWO HOURS AND A HALF TO DO THIS TEST
YOU MUST SHOW COMPLETE WORK ON ALL PROBLEMS

1- A high-level model for an LRU (Least Recently Used) indicator is to be developed. The LRU indicator ha 16 inputs from its 16 sources. These sources are memory pages (0 to 15) that inform the LRU indicator that they have been accessed. Based on when pages have been accessed, the LRU indicator produces the ID of the page that has been least recently used.
   A) Using a resolution function, write a high-level description for the LRU indicator.
   B) Encoding a page address indicates when a page is accessed, i.e., $accessed_i$. Use this signal to provide necessary information to the input of the LRU indicator



2- A number of devices (master) that require access to a certain shared resource make their requests from an Arbitrator, based on the priorities given to them a Priority Dispatcher. A master device wanting to use the shared resource, first obtains a priority from the Priority Dispatcher. Each master has a request input that stays active until the master has completed its operation. The Priority Dispatcher receiving a request issues a priority that is picked up by the master, and at the same time allows master connection to the arbiter.
The master has the option to hold on to the priority given to it and use it at a later time. For this, master has to keep its request active. However, the Priority Dispatcher may decide to disconnect a master based on some delay policy that it uses.

A) Write the interface of the Priority Dispatcher (ENTITY).
B) Show a block diagram and partial state machine of a master device.
C) Using a resolution function and connection/disconnection implement the Arbiter. The Arbiter produces all-zero [0:0] if no device is given access to the shared resource.



3- The formula below shows how to calculate *ln*(x). An RTL module for *ln*(x) is to be designed with the following parameters: An 8-bit fractional input *X*, an 8-bit fractional output *FractionalPart*, a 3-bit integer *IntegerPart* output, and an output *Sign* bit. Use *Start* and *Done* signals for a basic communication handshaking.

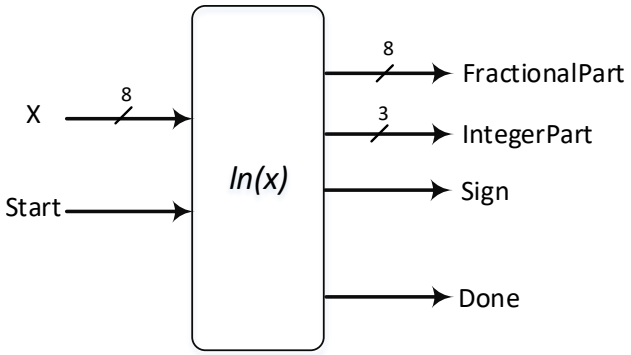
A) Draw the complete diagrams for the top-level module, the datapath, and the controller.

B) Write VHDL descriptions of the RTL components used in your design, the datapath, the controller, and the top-level module.

C) Write a testbench for your design.

$$ln(x) = \sum_{n=1}^{\infty} \left(\frac{(-1)^{n+1}}{n} (x-1)^n \right) = (x-1) - \frac{(x-1)^2}{2} + \frac{(x-1)^3}{3} - \cdots$$

$$\ldots for\ 0 \le x < 1$$



4- In the VHDL code shown below four processes generate drivers on w, x, y, and z signals. Show waveforms generated on these signals from time 0 to 20 NS. Consider sequential placement of transactions on signal drivers.

```
ENTITY placement IS END ENTITY;
ARCHITECTURE sequential OF placement IS

   TYPE four IS (V1, V2, V3, V4);
   SIGNAL w, x, y, z : four;

BEGIN

  w <= V1 AFTER 5 NS, V4 AFTER 9 NS;

  x <= V3, V2 AFTER 3 NS, V3 AFTER 8 NS, V4 AFTER 12 NS;

  y <= V2, W AFTER 2 NS, x AFTER 4 NS;

  z <= TRANSPORT W AFTER 2 NS, x AFTER 4 NS;

END sequential;
```