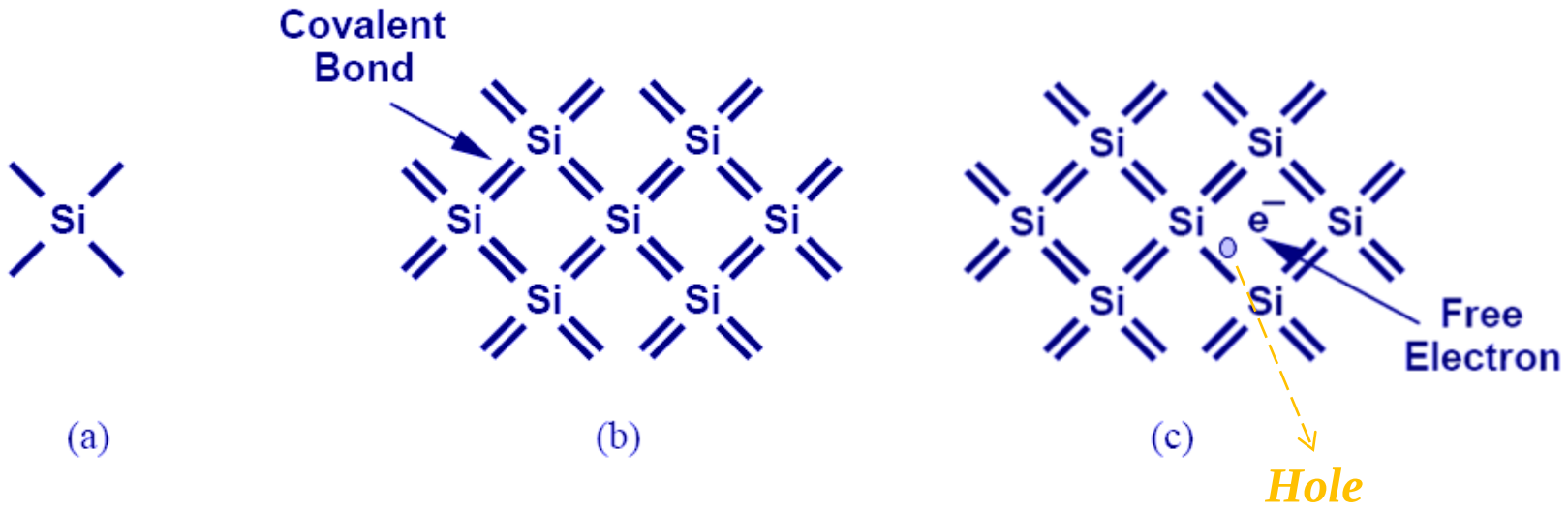

بسم الله الرحمن الرحیم

Course Overview

الکترونیک ۱

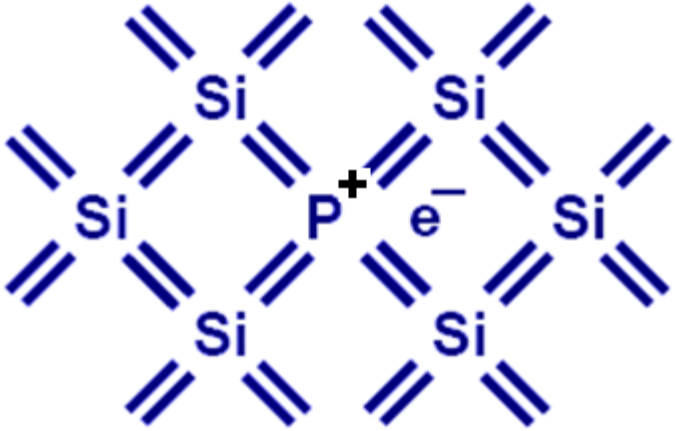
- Semiconductor physics
- PN junction
- BJT physics
- BJT Model
- MOSFET

Silicon



- Si has four valence electrons. Therefore, it can form covalent bonds with four of its neighbors.
- When temperature goes up, electrons in the covalent bond can become free.
- E_g, or bandgap energy determines how much effort is needed to break off an electron from its covalent bond.

Doping (N type)



Free electron density: n

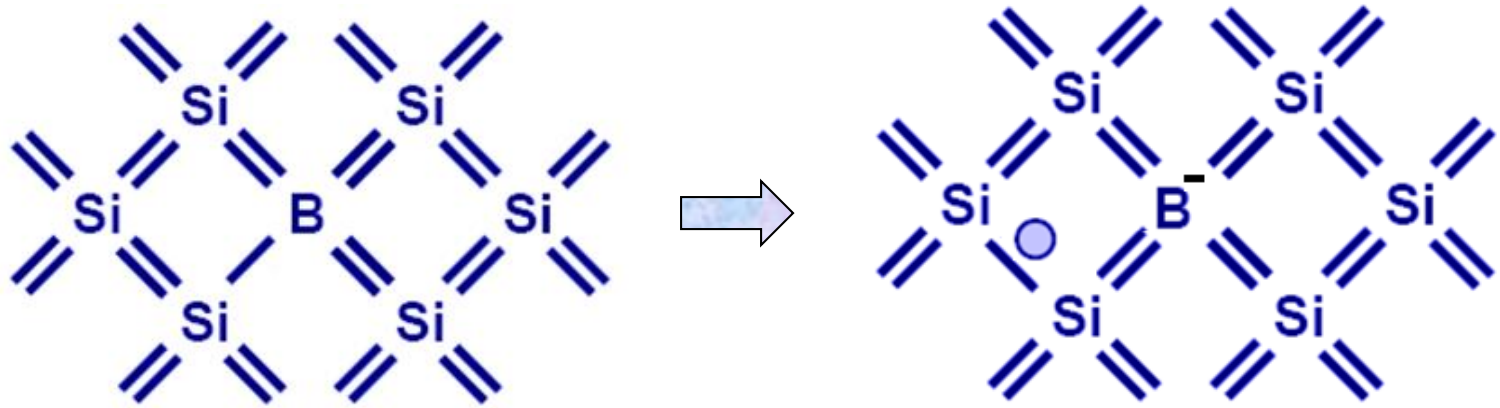
Hole density: p

Donor concentration: N_d

$$n = p + N_d$$

- Pure Si can be doped with other elements to change its electrical properties.
- For example, if Si is doped with group-V elements such as P (phosphorous), then it has more electrons, or becomes type N (electron).
- Group-V impurities are called Donors
- electron: majority carrier

Doping (P type)



- If Si is doped with group-III elements such as B (boron), then it has more holes, or becomes type P. hole: majority carrier
- Group-III impurities are called Acceptors.

Free electron density: n

Hole density: p

Acceptor concentration: N_a

$$n + N_a = p$$

Electron and Hole Densities

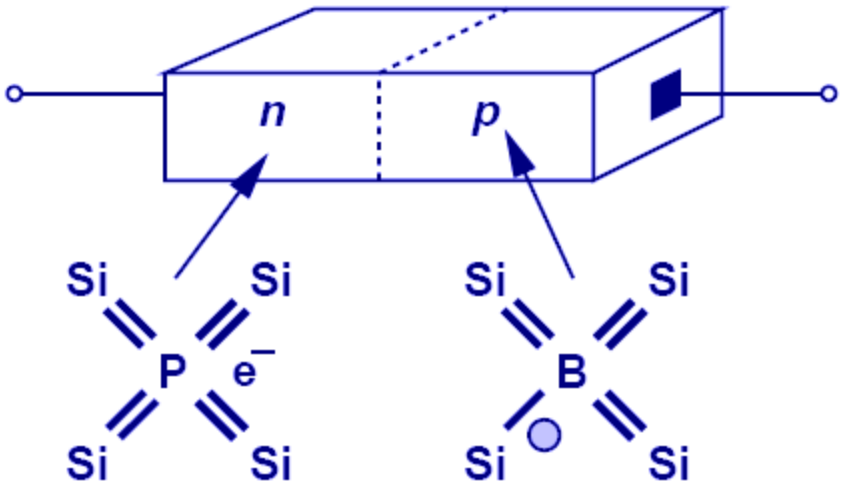
- The product of electron and hole densities is ALWAYS equal to the square of intrinsic electron density regardless of doping levels.

$$n.p=n_i^2 \qquad \textit{:Mass Action Law}$$

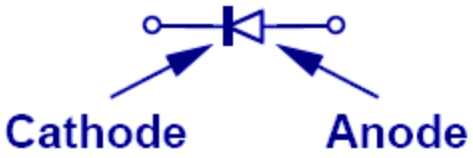
$$n+N_a=p+N_d$$

	Majority Carrier Conc.	Minority Carrier Conc. (Mass Action Law)
N-Type	$n \approx N_d$	$p=n_i^2/n$
P-Type	$p \approx N_a$	$n=n_i^2/p$

PN Junction (Diode)



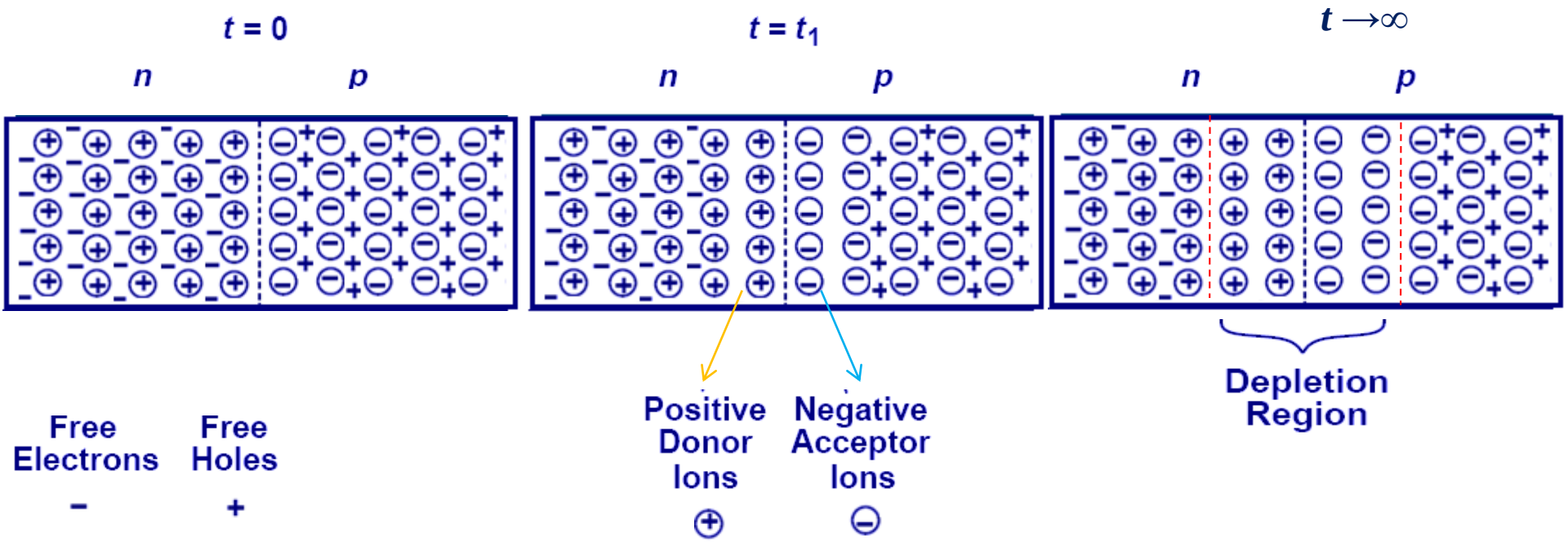
(a)



(b)

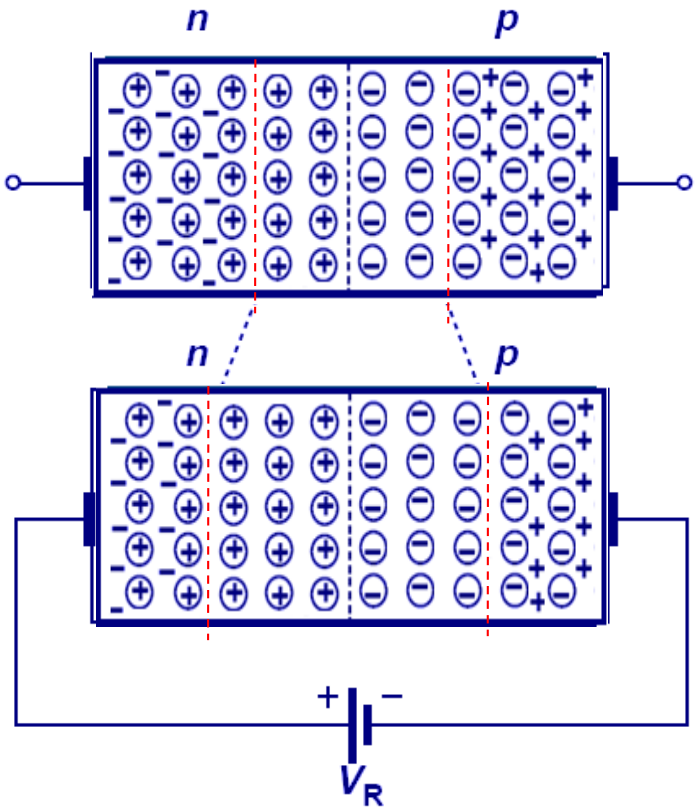
- When N-type and P-type dopants are introduced side-by-side in a semiconductor, a PN junction or a diode is formed.

Depletion Region



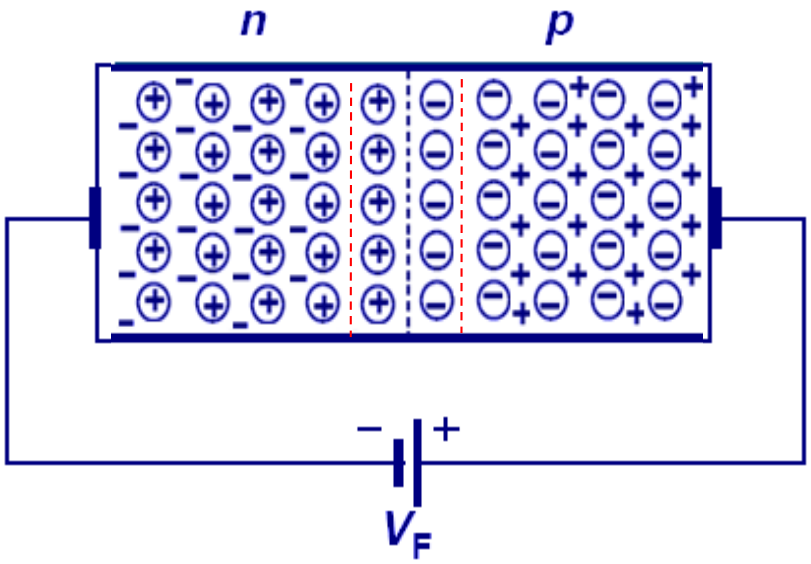
- As free electrons and holes diffuse across the junction, a region of fixed ions is left behind. This region is known as the "depletion region."

Diode in Reverse Bias



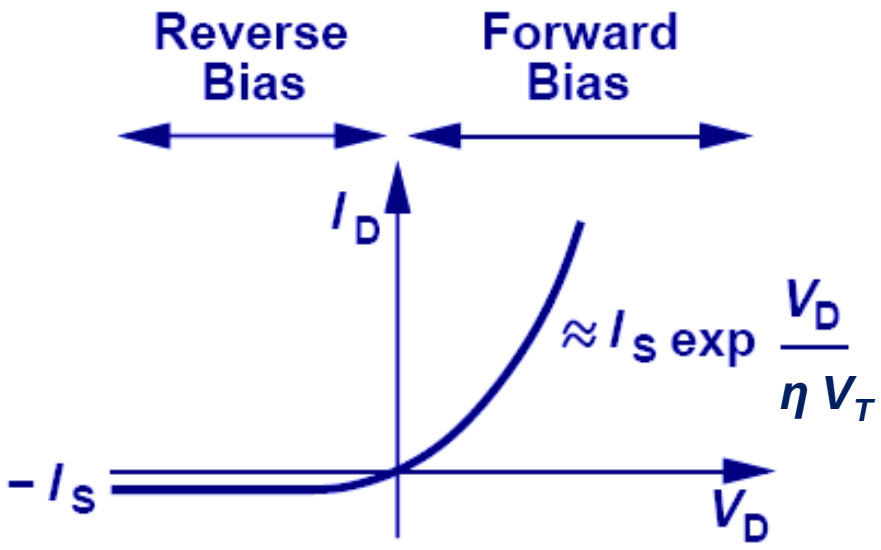
- When the N-type region of a diode is connected to a higher potential than the P-type region, the diode is under reverse bias, which results in wider depletion region and larger built-in electric field across the junction.

Diode in Forward Bias



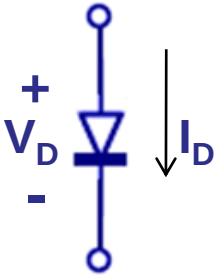
- When the N-type region of a diode is at a lower potential than the P-type region, the diode is in forward bias.
- The depletion width is shortened and the built-in electric field decreased.

IV Characteristic of PN Junction



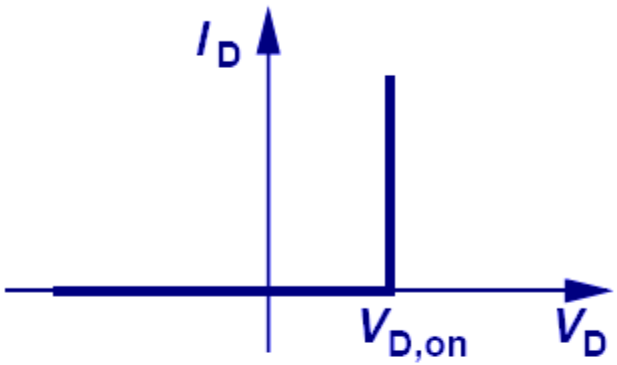
$$I_D = I_S (\exp \frac{V_D}{\eta V_T} - 1)$$

$$I_s = Aqn_i^2 (\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p})$$

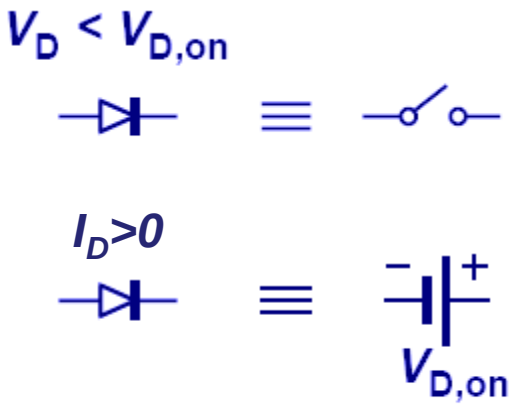


- The current and voltage relationship of a PN junction is exponential in forward bias region, and relatively constant in reverse bias region.

Constant-Voltage Diode Model

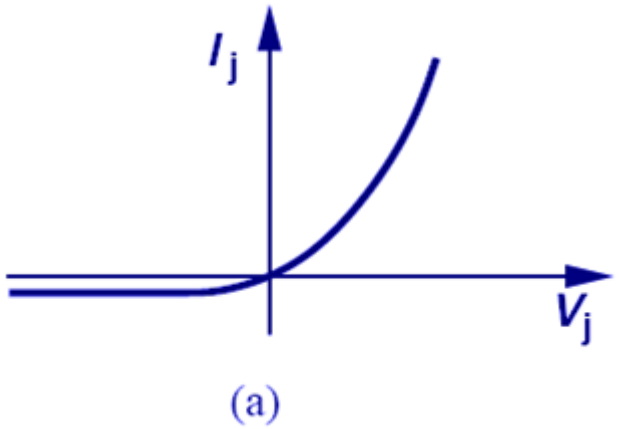


(a)



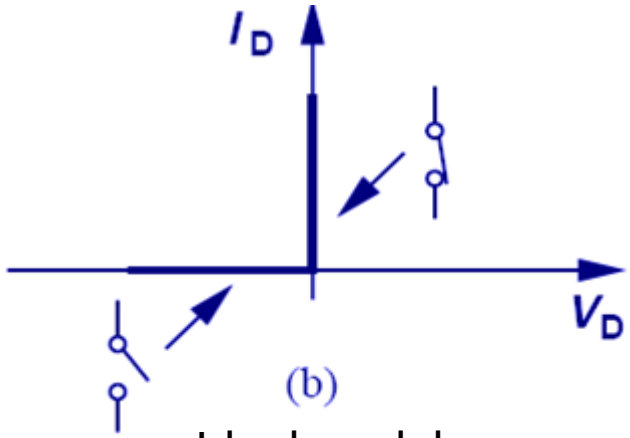
(b)

Different Models for Diode



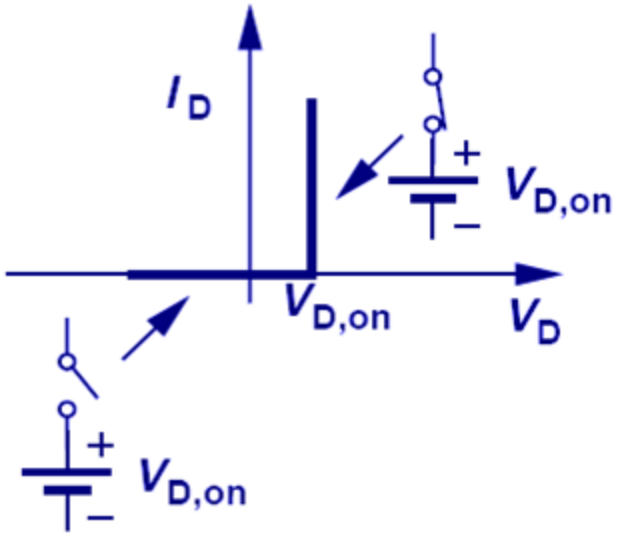
(a)

Exponential model

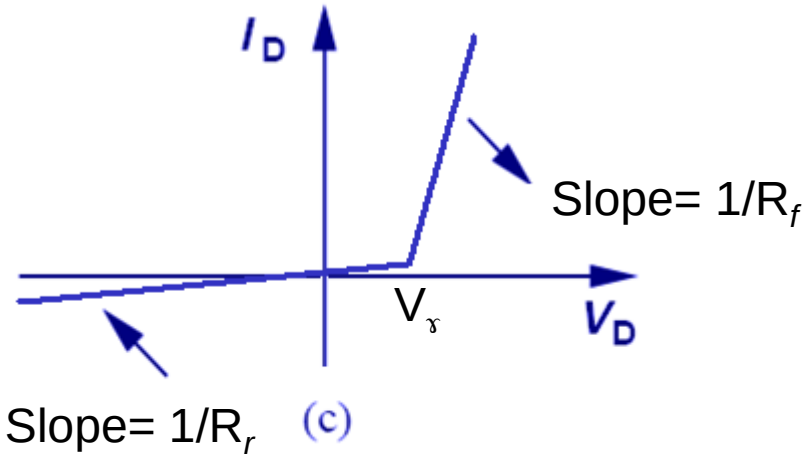


(b)

Ideal model



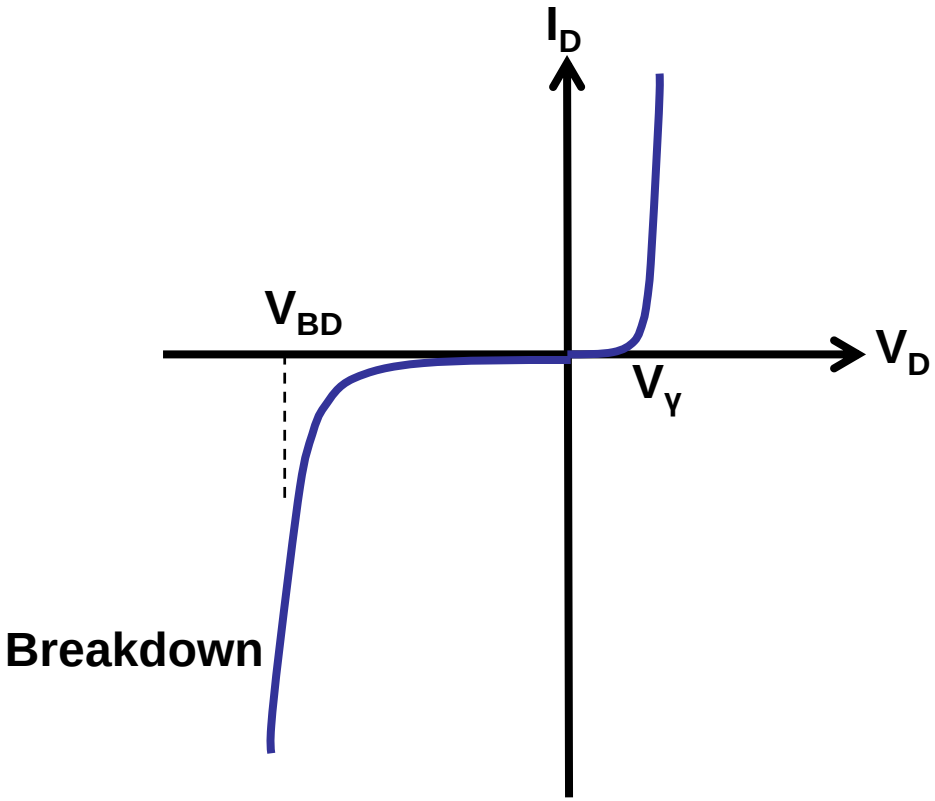
constant voltage model



(c)

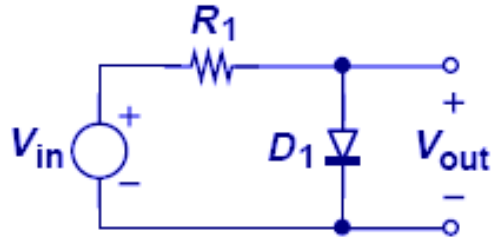
Piece-wise linear model

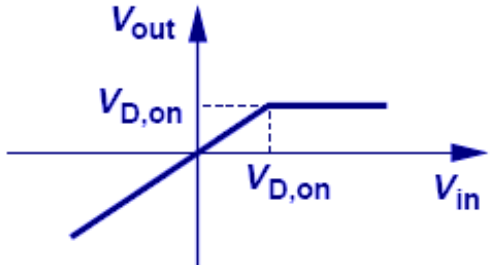
Reverse Breakdown



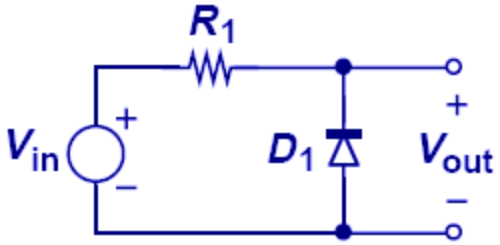
- When a large reverse bias voltage is applied, breakdown occurs and an enormous current flows through the diode.

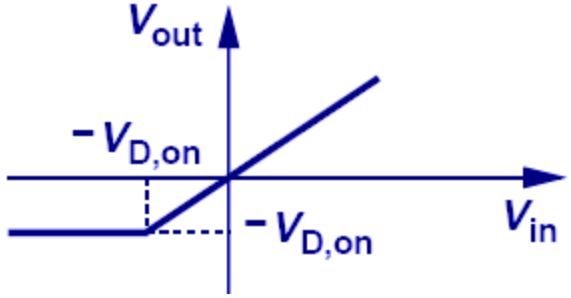
Limiting Circuit Using Diode:



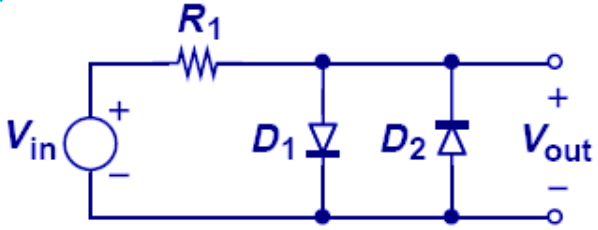


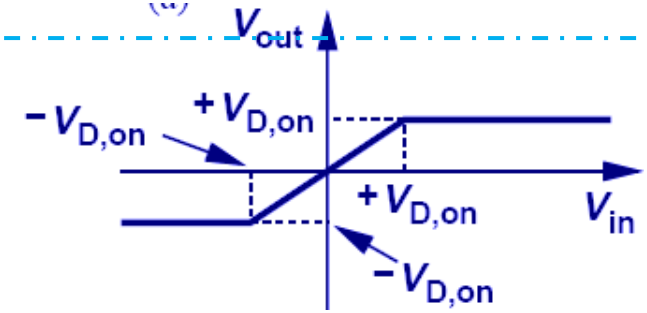
- Positive Cycle Clipping





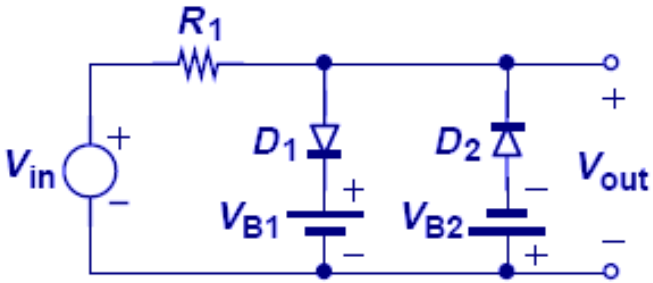
Negative Cycle Clipping

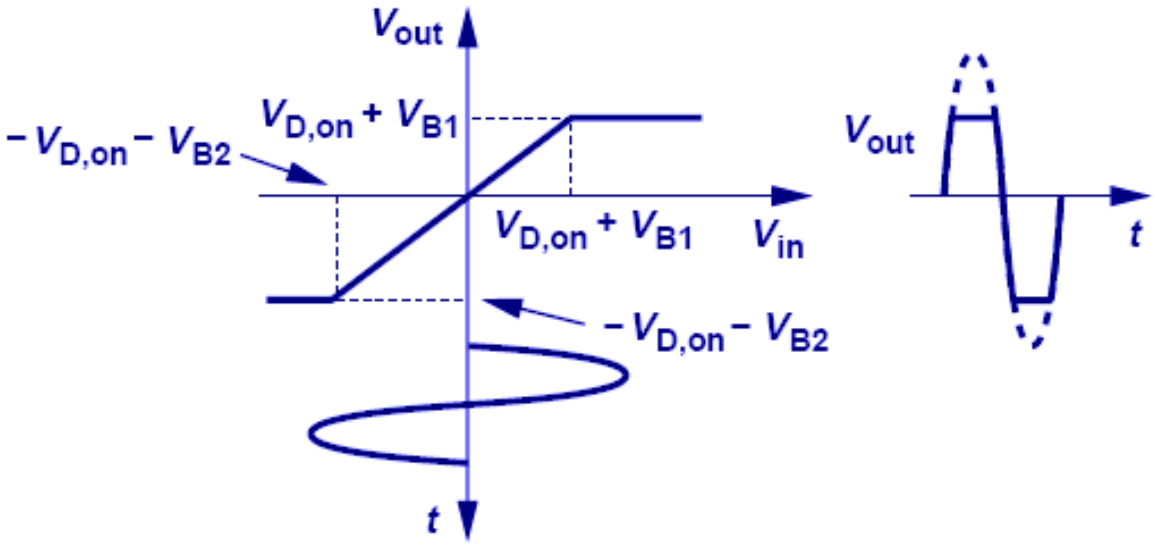




Positive and Negative Cycle Clipping

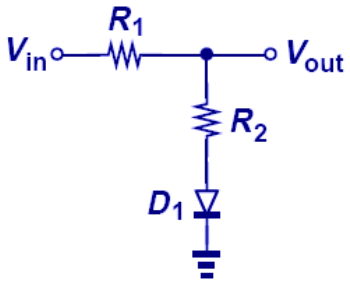
General Voltage Limiting Circuit

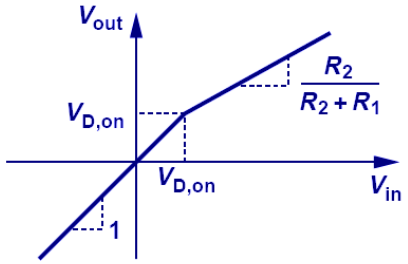


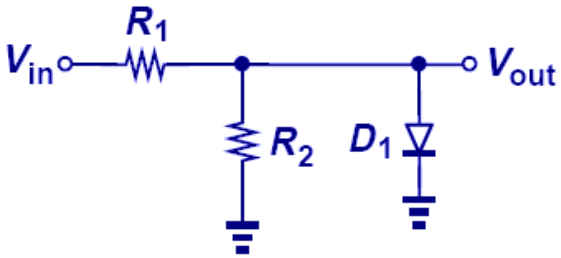


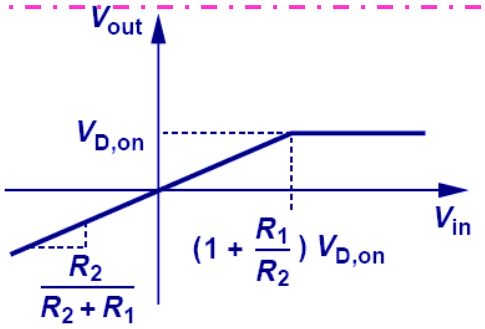
- Two batteries in series with the antiparalle diodes control the limiting voltages.

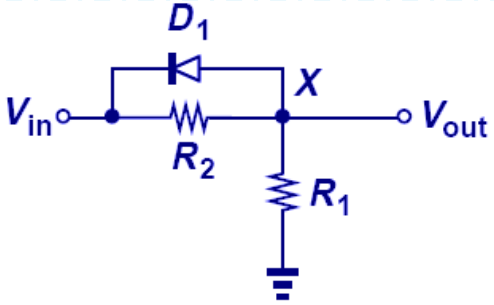
Input/Output Characteristics with Ideal and Constant-Voltage Models

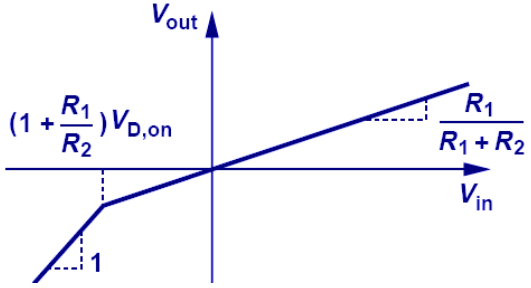




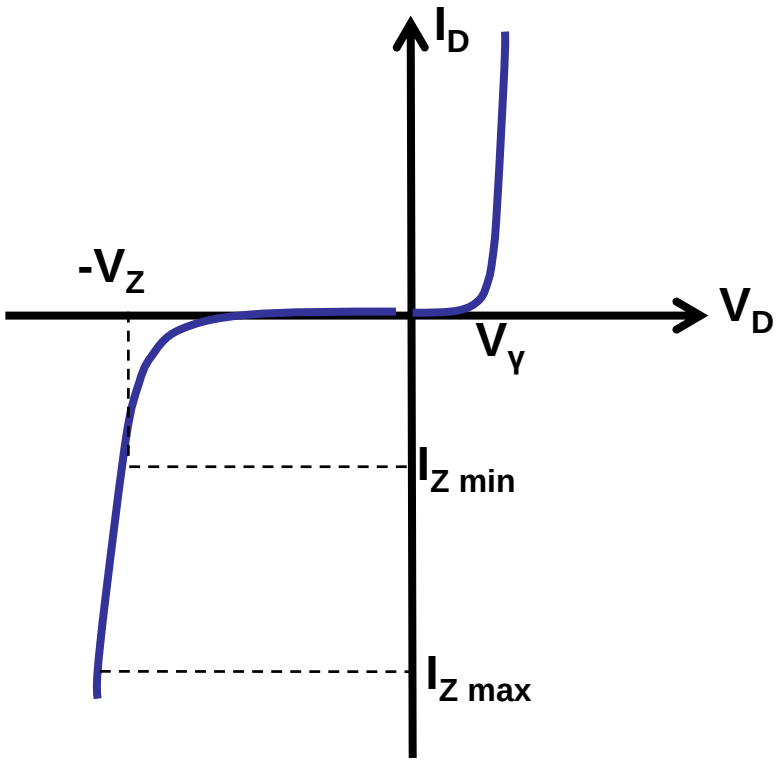


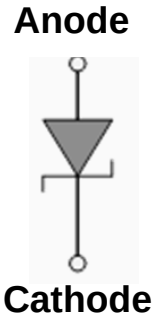




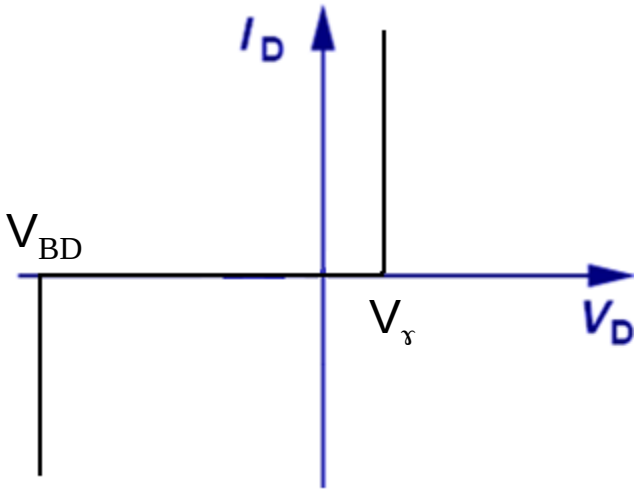


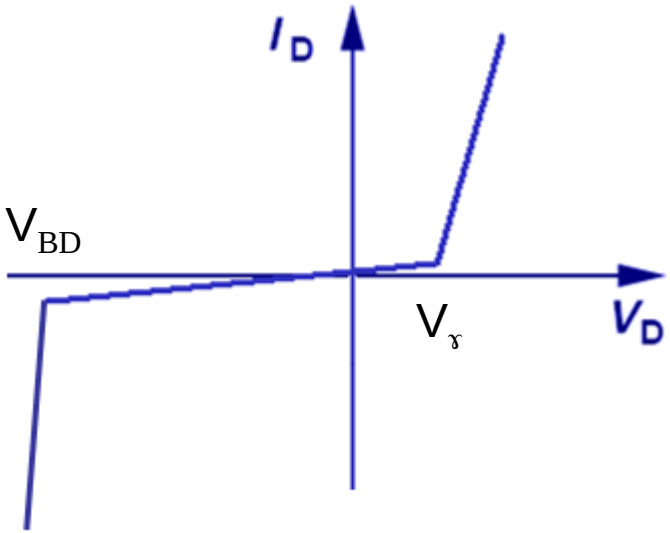
Zener Diode



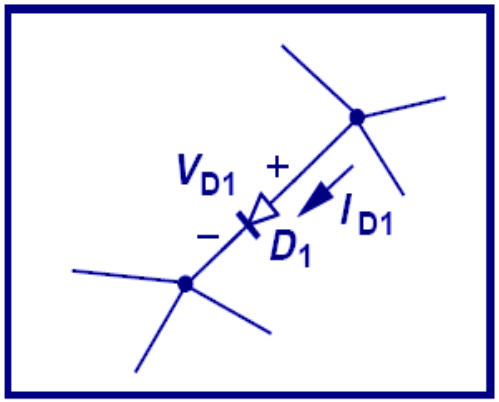


Zener Diode: Models

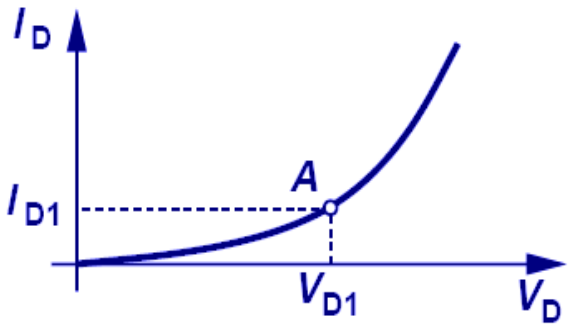




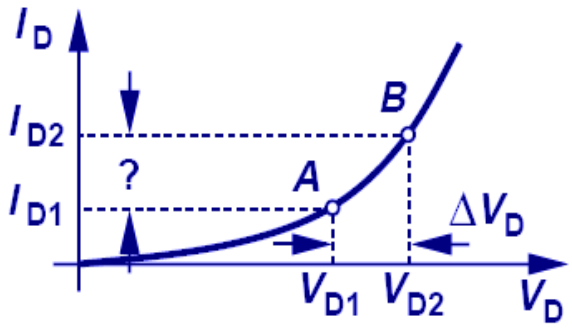
Small-Signal Analysis



(a)



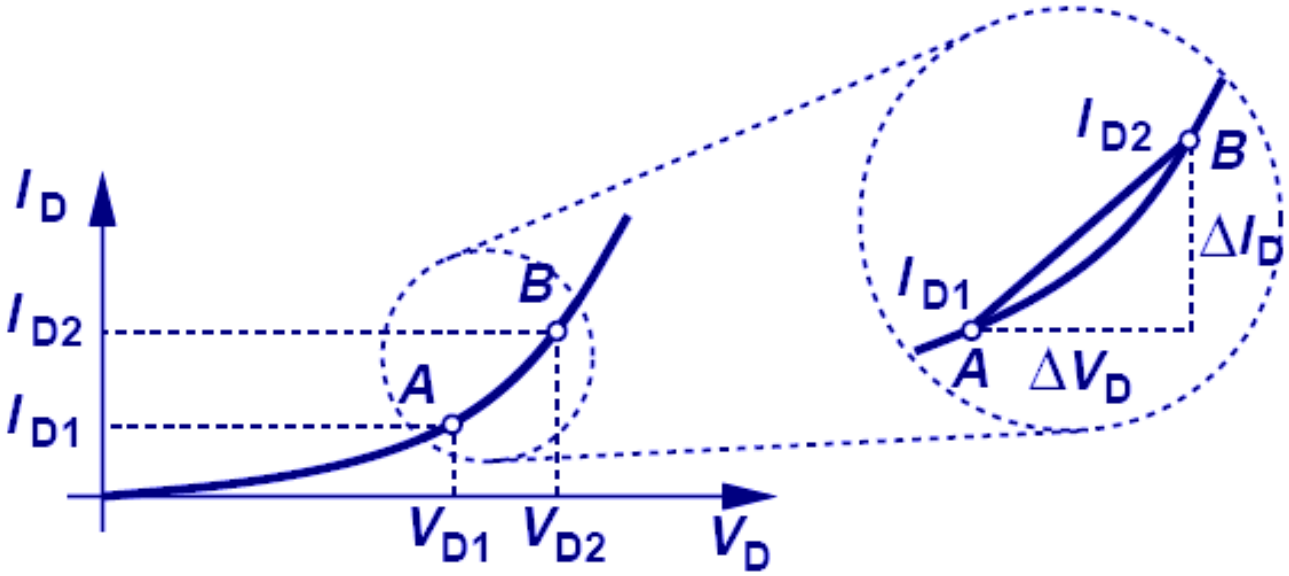
(b)



(c)

- Small-signal analysis is performed around a bias point by perturbing the voltage by a small amount and observing the resulting linear current perturbation.

Small-Signal Analysis in Detail



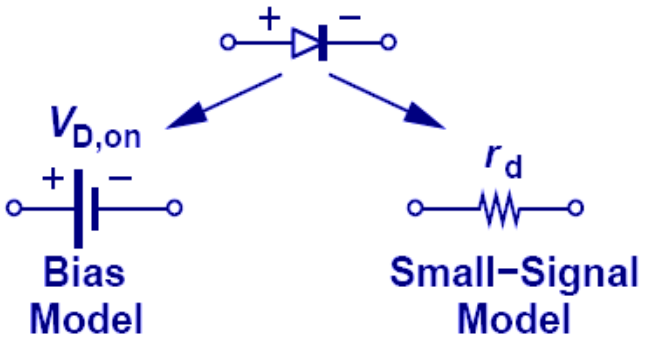
$$\frac{\Delta I_D}{\Delta V_D} = \frac{dI_D}{dV_D}\Big|_{VD=VD1}$$

$$= \frac{I_s}{\eta V_T}\exp\frac{I_{D1}}{\eta V_T}$$

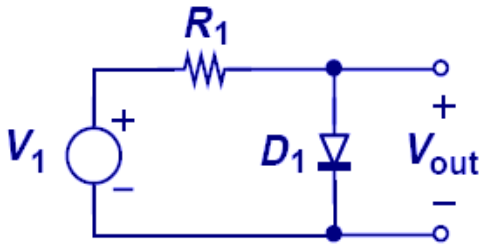
$$= \frac{I_{D1}}{\eta V_T}$$

- If two points on the IV curve of a diode are close enough, the trajectory connecting the first to the second point is like a line, with the slope being the proportionality factor between change in voltage and change in current.

Small-Signal Incremental Resistance



(a)



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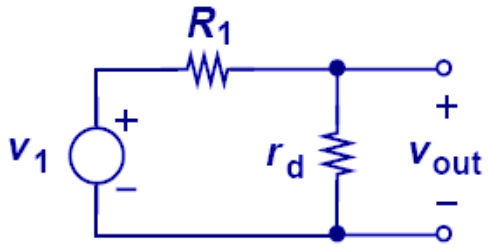
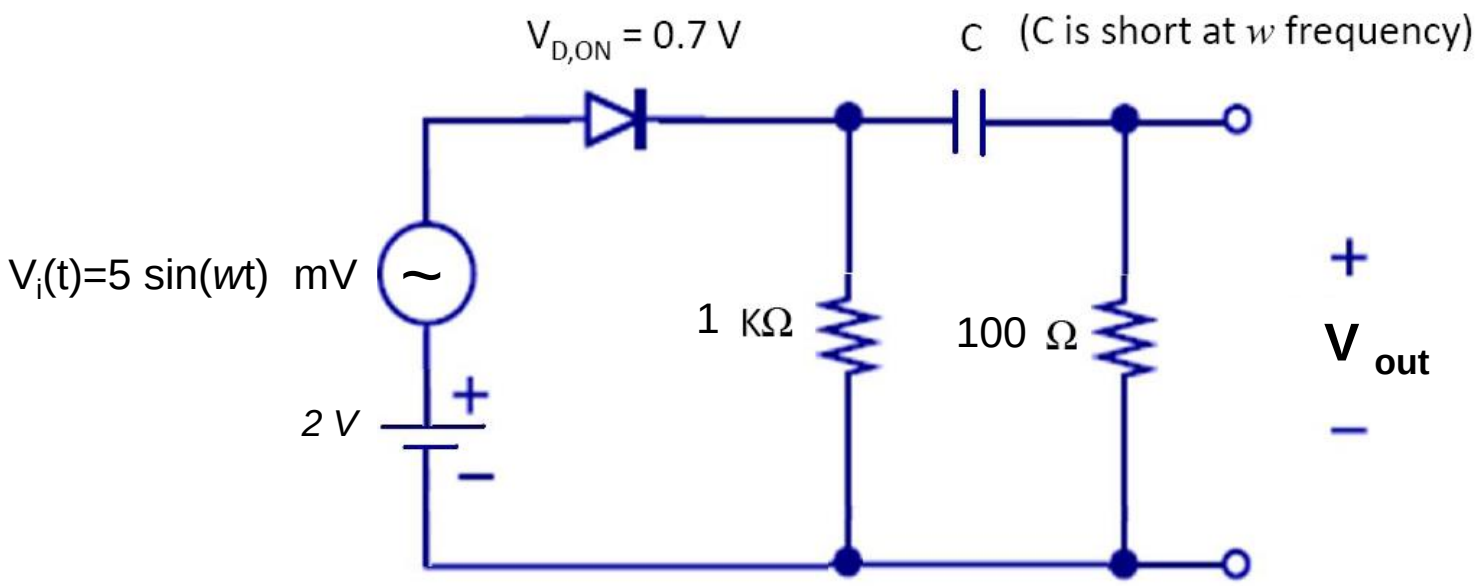


(c)

$$r_d = \frac{\eta V_T}{I_D}$$

- Since there's a linear relationship between the small signal current and voltage of a diode, the diode can be viewed as a linear resistor when only small changes are of interest.

Example: Small-Signal Analysis



η=1.4
$V_{D\ on}$=0.7 V

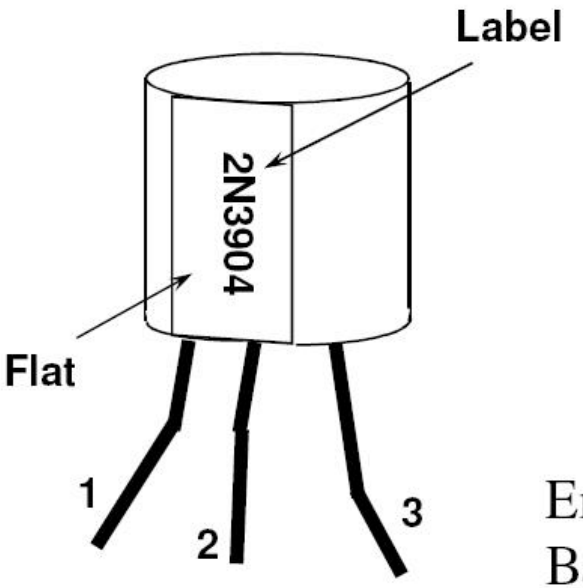
r_d=27 Ω
$V_{out\ ac}$=91/118 V_i=0.77 $V_i(t)$

Course Overview

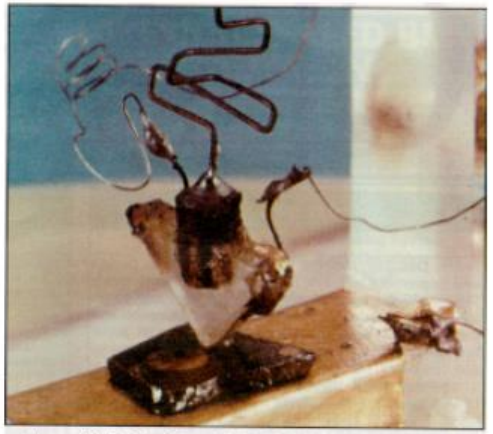
الکترونیک ۱

- Semiconductor physics ✓
- PN junction
  - Physics
  - dc analysis ✓
  - ac analysis
- BJT physics ⬅
- BJT Model
- Amplifiers
- MOSFET

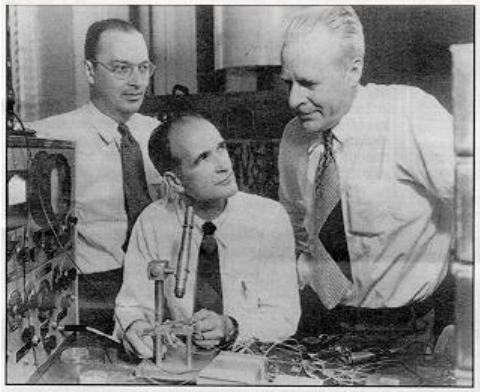
Bipolar Transistor



Emitter
Base
Collector

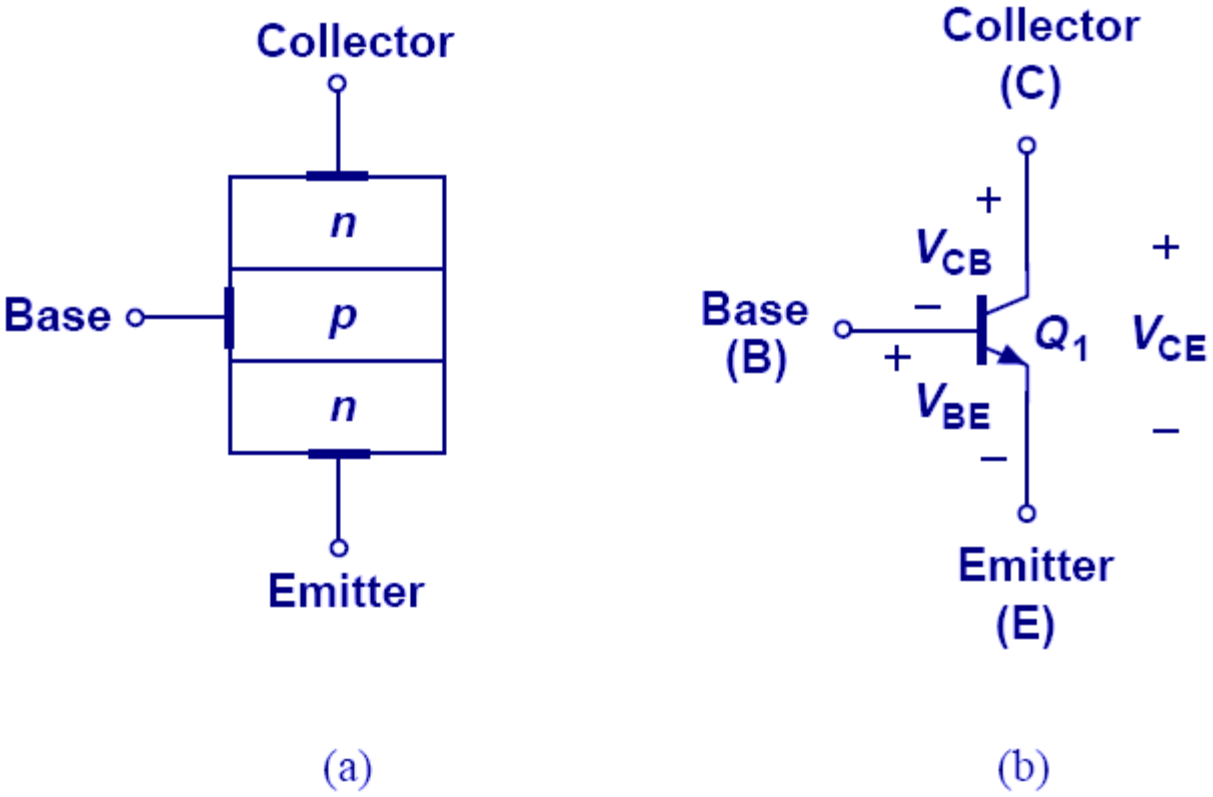


The world's first transistor, built at Bell Labs in December, 1947.



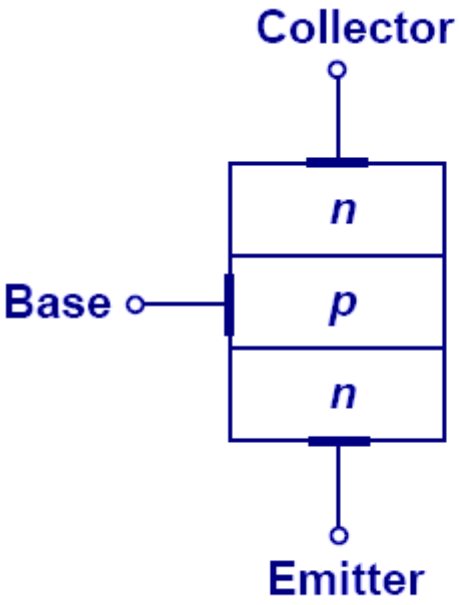
Transistor inventors (from left), Dr. Walter Brattain, Dr. William Shockley, and Dr. John Bardeen.

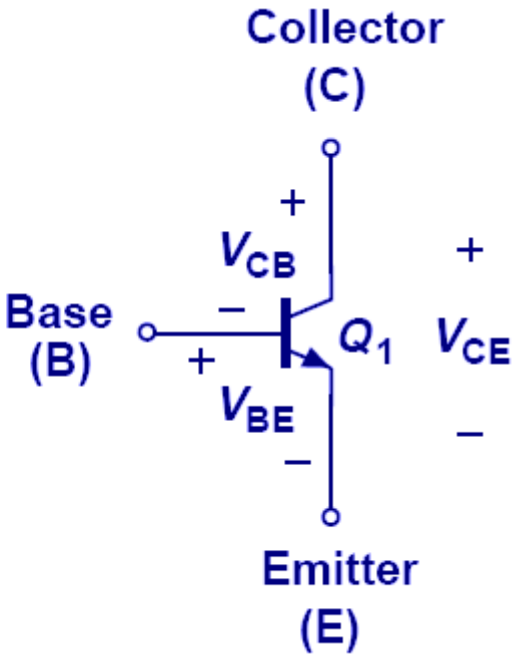
Structure and Symbol of Bipolar Transistor



- Bipolar transistor can be thought of as a sandwich of three doped Si regions. The outer two regions are doped with the same polarity, while the middle region is doped with opposite polarity.

Structure and Symbol of Bipolar Transistor

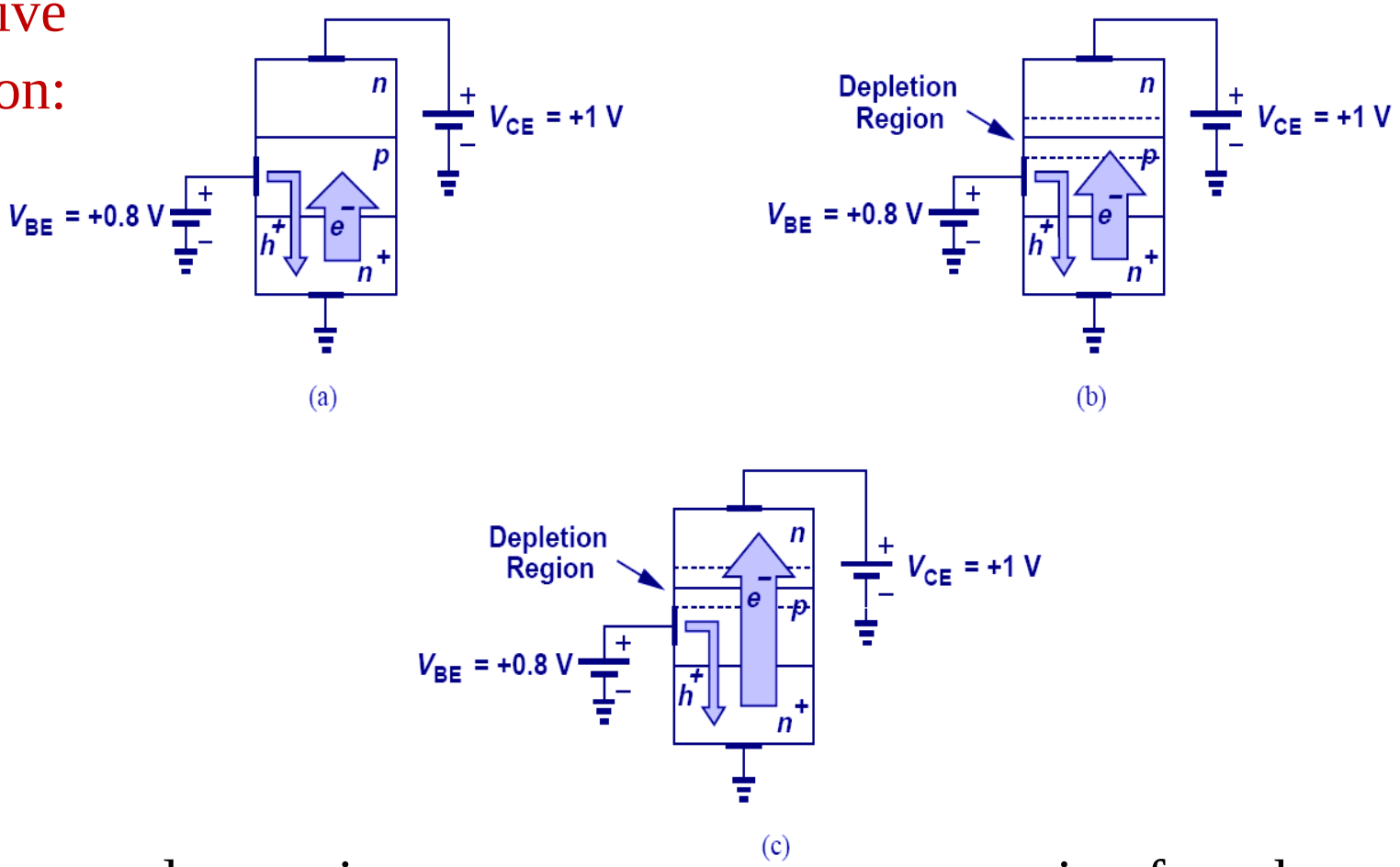




Base-Emitter	Collector-Base	Transistor Mode
FB	RB	Forward active
FB	FB	Saturation
RB	RB	Off

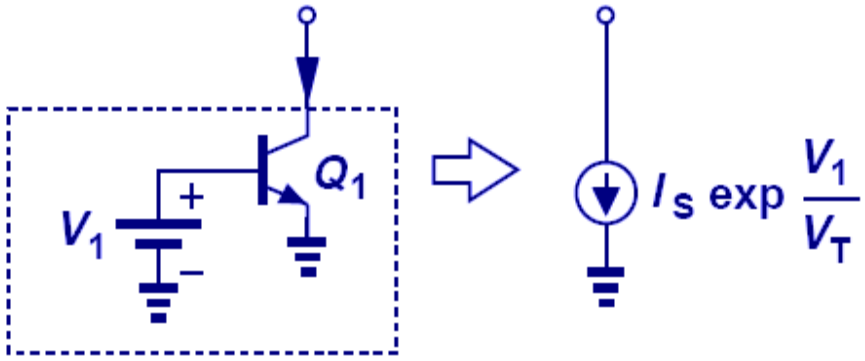
Accurate Bipolar Representation

In Active region:

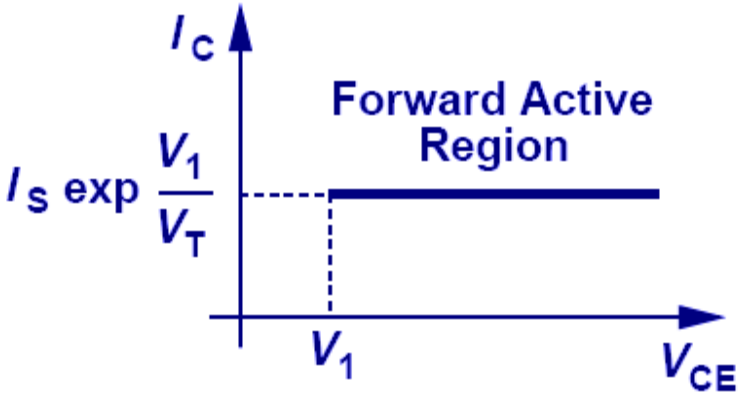


- Collector also carries current due to carrier injection from base.

Constant Current Source



(a)



(b)

- Ideally, the collector current does not depend on the collector to emitter voltage. This property allows the transistor to behave as a constant current source when its base-emitter voltage is fixed.

Currents

Always: ✓ $I_E = I_C + I_B$

In Active region:

$$I_E = \frac{I_C}{\alpha}$$

$$I_B = \frac{I_C}{\beta}$$

$$\frac{\beta}{\beta+1} = \alpha$$

$$\frac{\alpha}{1-\alpha} = \beta$$

- Applying KCL to the transistor, we can easily find the emitter current.

β, α

$$\frac{\beta}{\beta+1}=\alpha$$

$$\frac{\alpha}{1-\alpha}=\beta$$

β	α
9	0.9
19	0.95
99	0.99
499	0.998

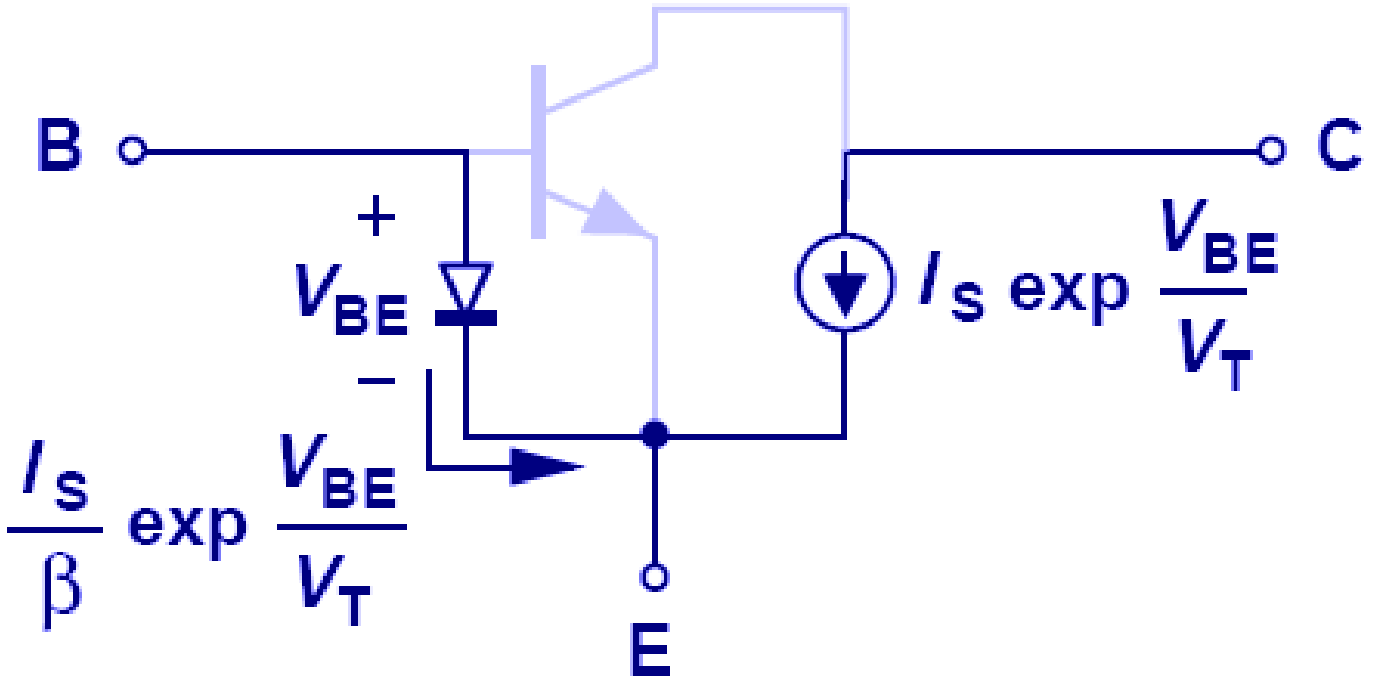
$$10 \le \beta \le 500$$

Typically:

$$0.9 \le \alpha < 1$$

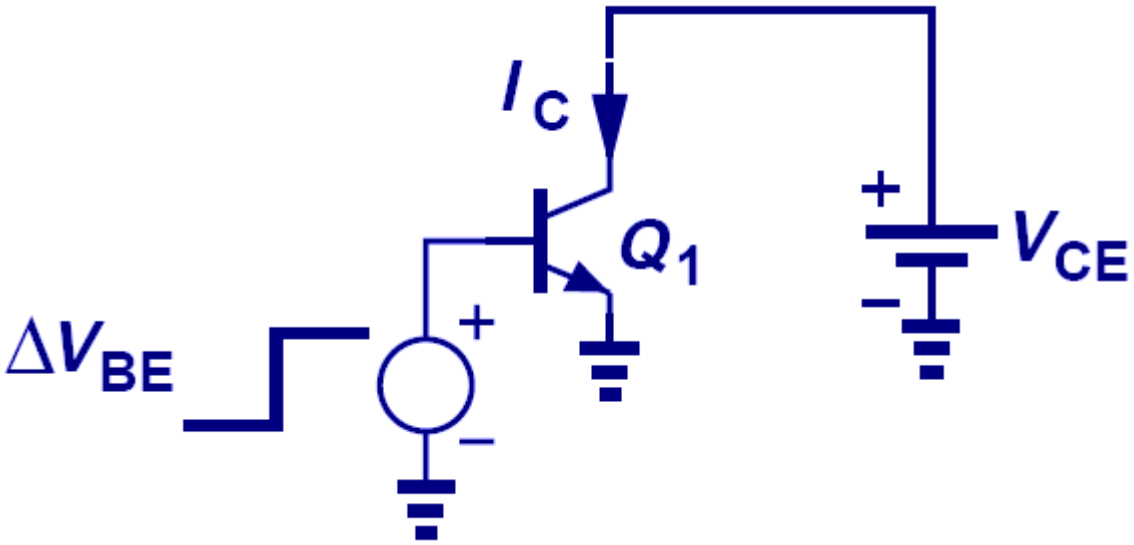
Bipolar Transistor Large Signal Model

In Active region:



- A diode is placed between base and emitter and a voltage controlled current source is placed between the collector and emitter.

Transconductance



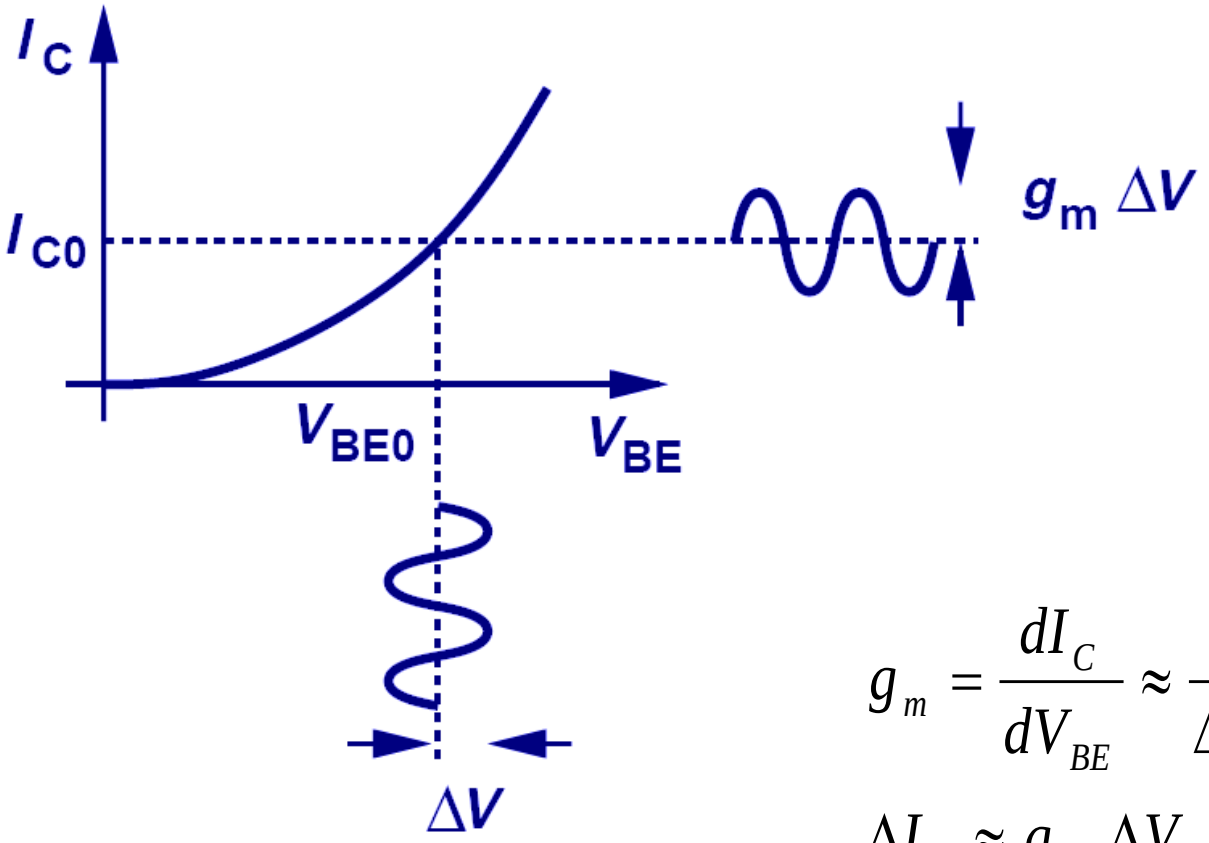
$$g_m = \frac{d}{dV_{BE}}\left(I_S \exp\frac{V_{BE}}{V_T}\right)$$

$$g_m = \frac{1}{V_T} I_S \exp\frac{V_{BE}}{V_T}$$

$$g_m = \frac{I_C}{V_T}$$

- Transconductance, g_m shows a measure of how well the transistor converts voltage to current.
- It will later be shown that g_m is one of the most important parameters in circuit design.

Visualization of Transconductance

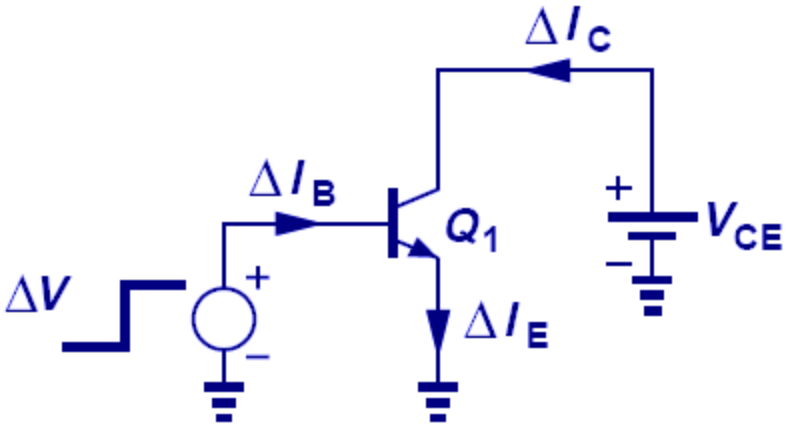


$$g_m = \frac{dI_C}{dV_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}} = \frac{I_C}{V_T}$$

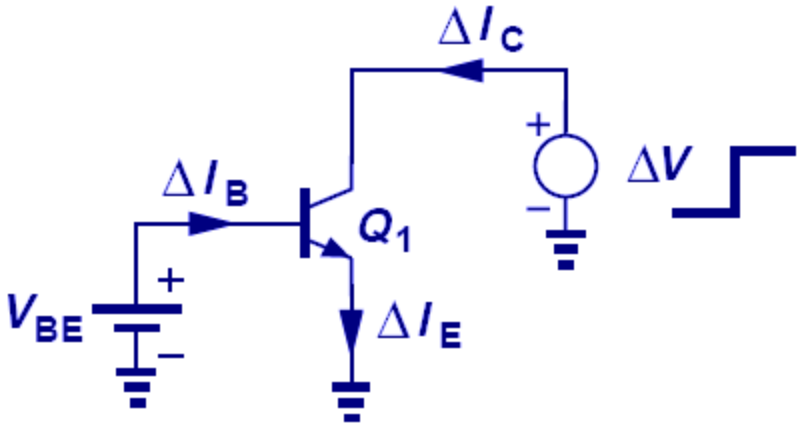
$$\Delta I_C \approx g_m . \Delta V_{BE}$$

- g_m can be visualized as the slope of I_C versus V_{BE}.
- A large I_C has a large slope and therefore a large g_m.

Small-Signal Model: Derivation



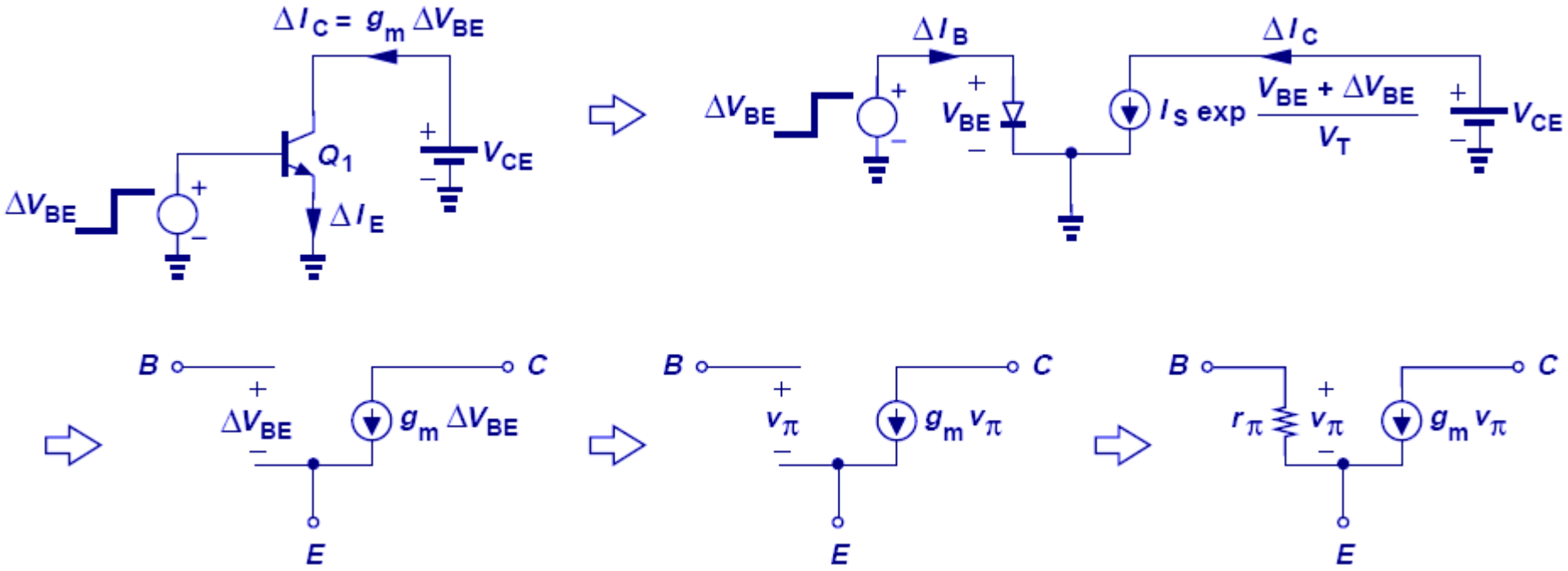
(a)



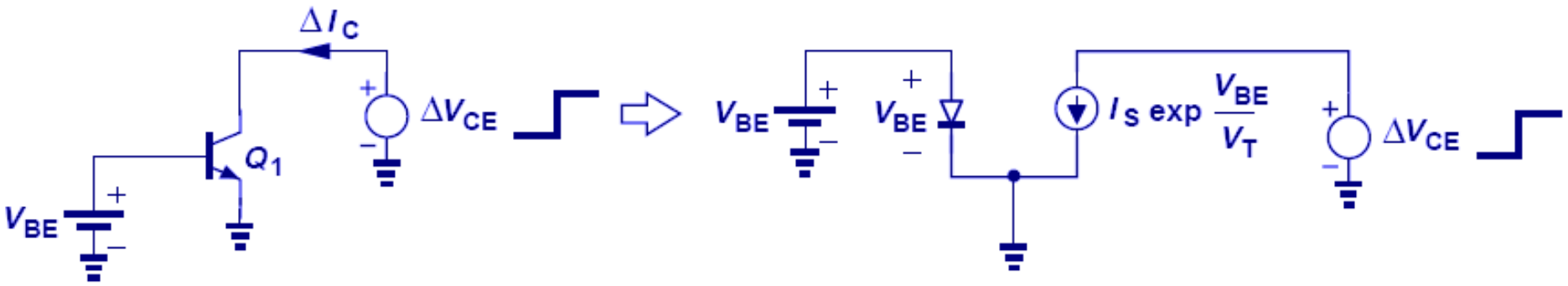
(b)

- Small signal model is derived by perturbing voltage difference every two terminals while fixing the third terminal and analyzing the change in current of all three terminals. We then represent these changes with controlled sources or resistors.

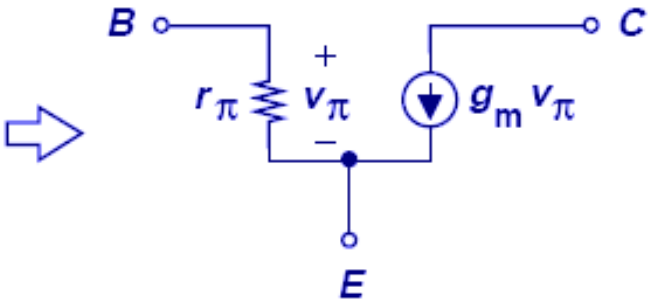
Small-Signal Model: V_{BE} Change



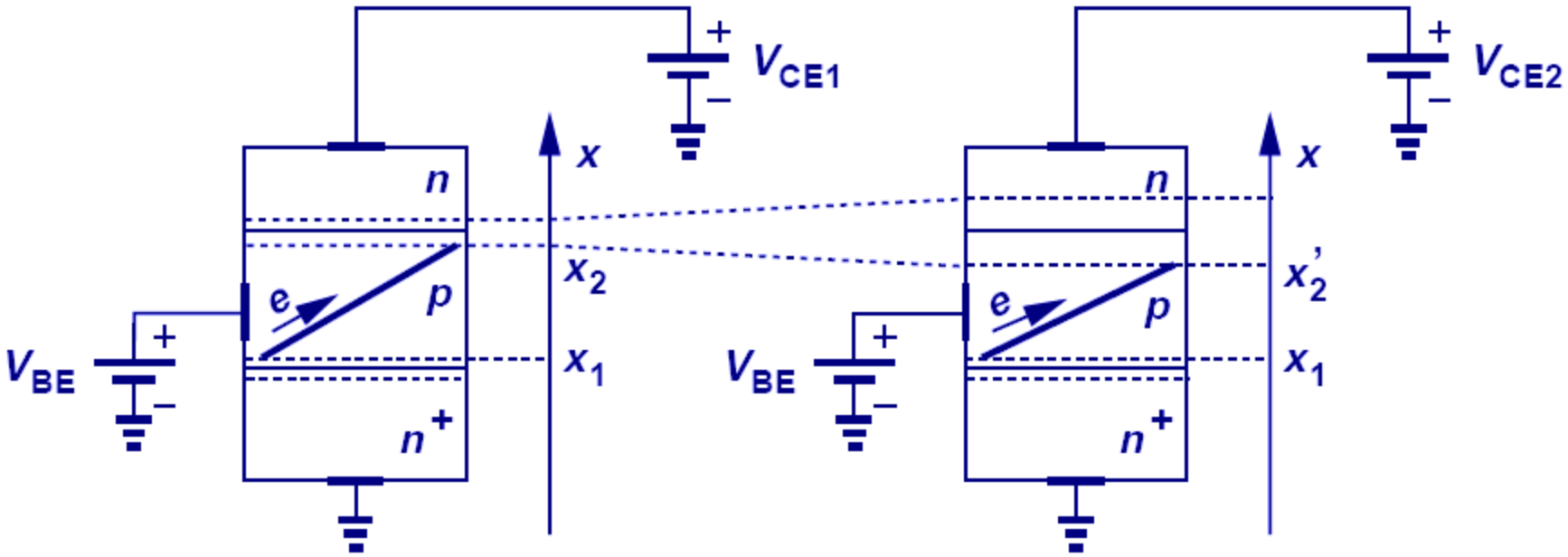
Small-Signal Model: V_{CE} Change



- Ideally, V_{CE} has no effect on the collector current. Thus, it will not contribute to the small signal model.
- It can be shown that V_{CB} has no effect on the small signal model, either.

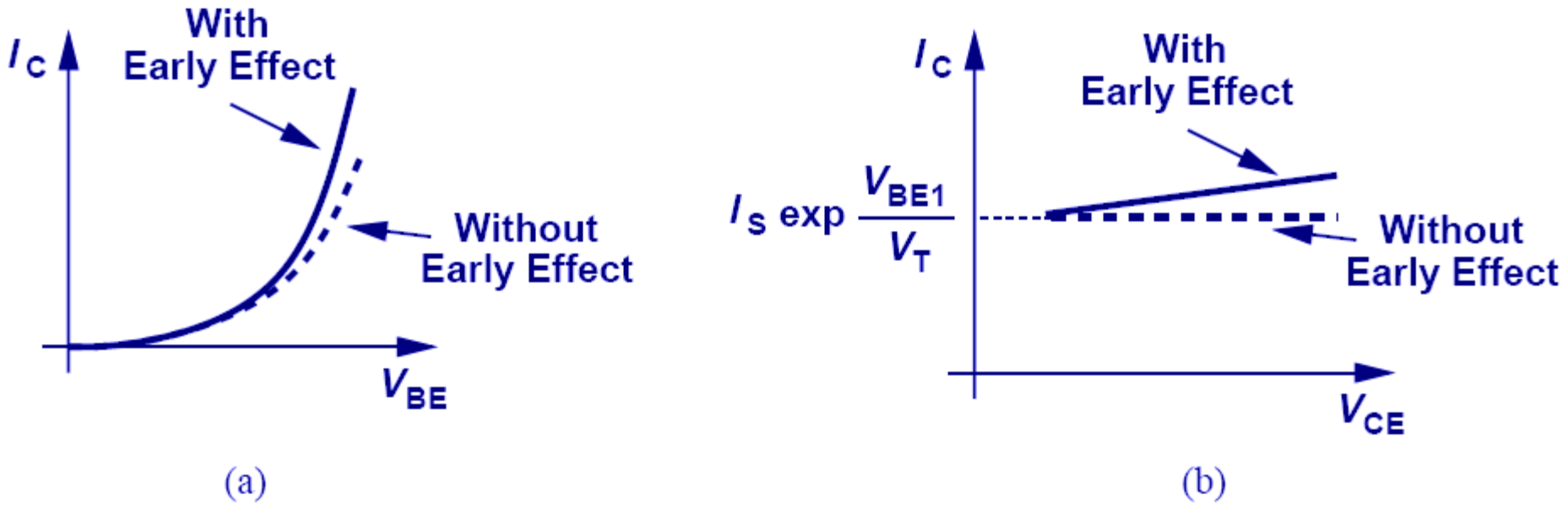


Early Effect



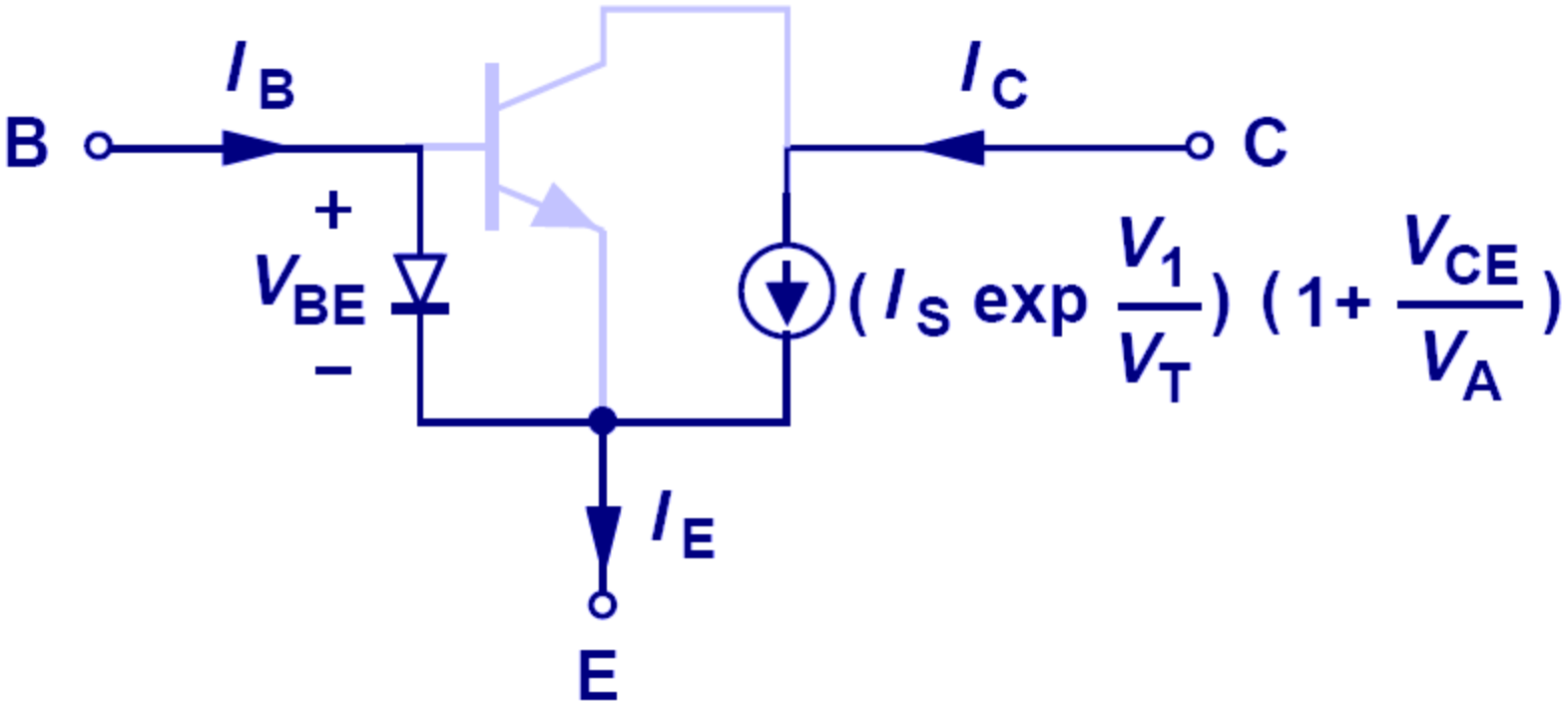
- The claim that collector current does not depend on V_{CE} is not accurate.
- As V_{CE} increases, the depletion region between base and collector increases. Therefore, the effective base width decreases, which leads to an increase in the collector current.

Early Effect Illustration



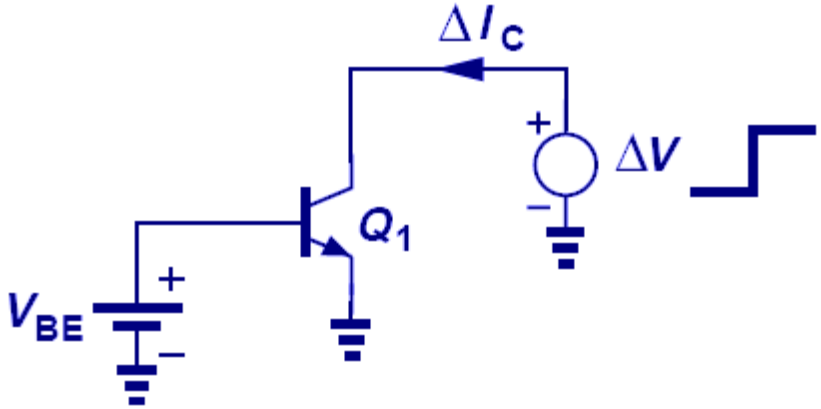
- With Early effect, collector current becomes larger than usual and a function of V_{CE}.

Early Effect and Large-Signal Model

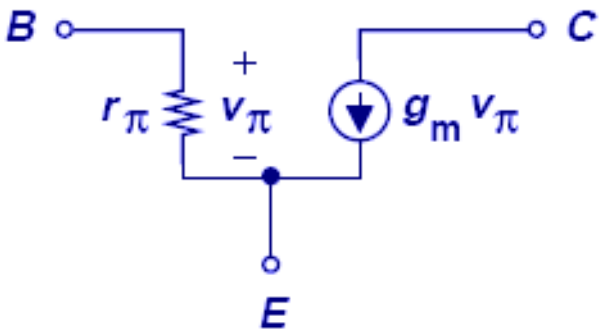


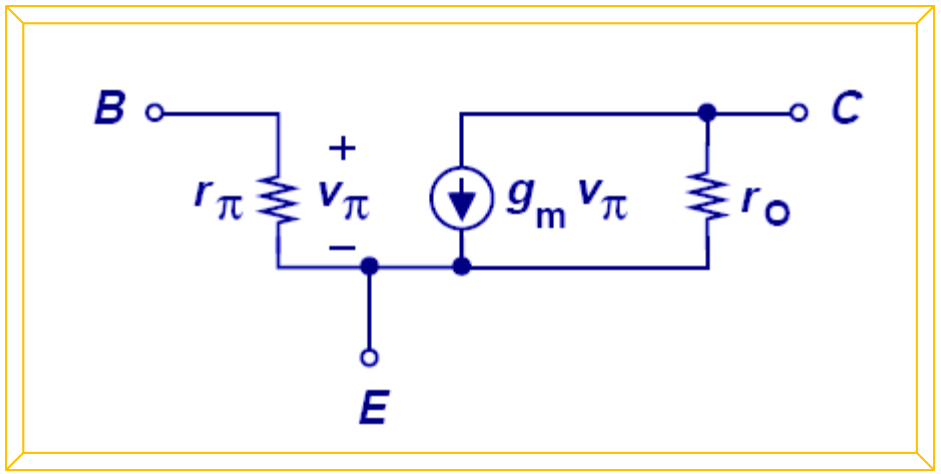
- Early effect can be accounted for in large-signal model by simply changing the collector current with a correction factor.
- In this mode, base current does not change.

Early Effect and Small-Signal Model



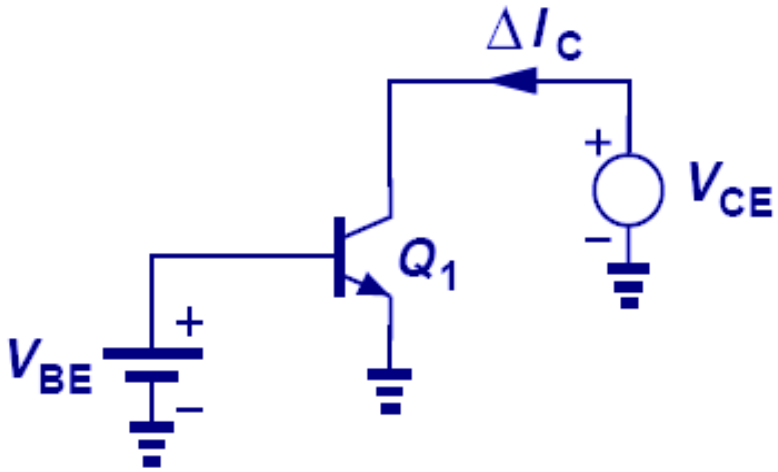
$$\frac{\Delta I_C}{\Delta V_{CE}} = \frac{I_S \exp \frac{V_{BE}}{V_T}}{V_A} \approx \frac{I_C}{V_A} = \frac{1}{r_o}$$





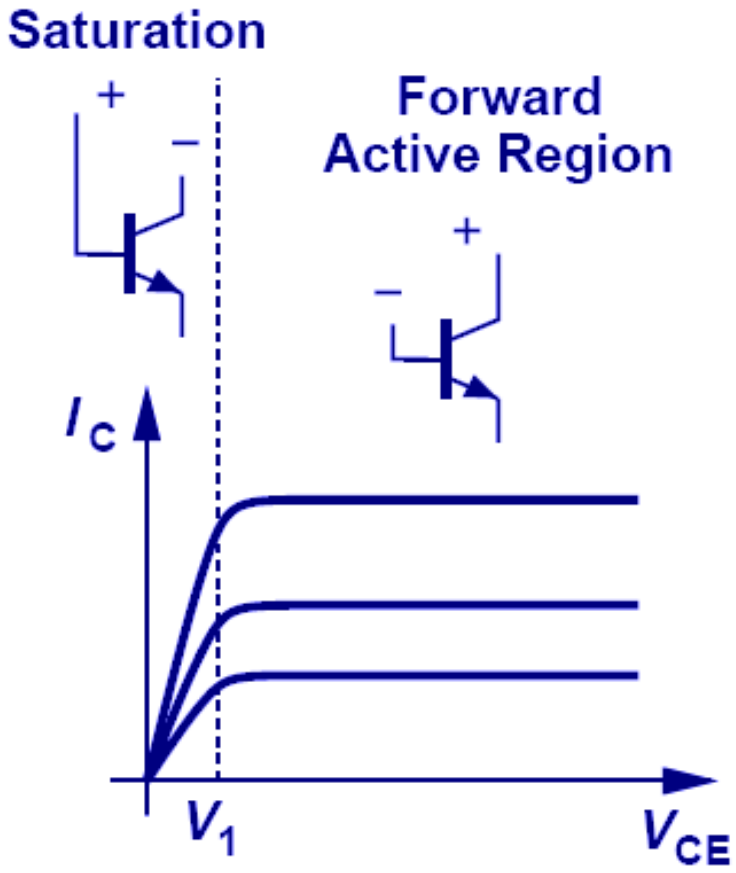
Small-Signal Model of BJT

Bipolar Transistor in “Saturation“

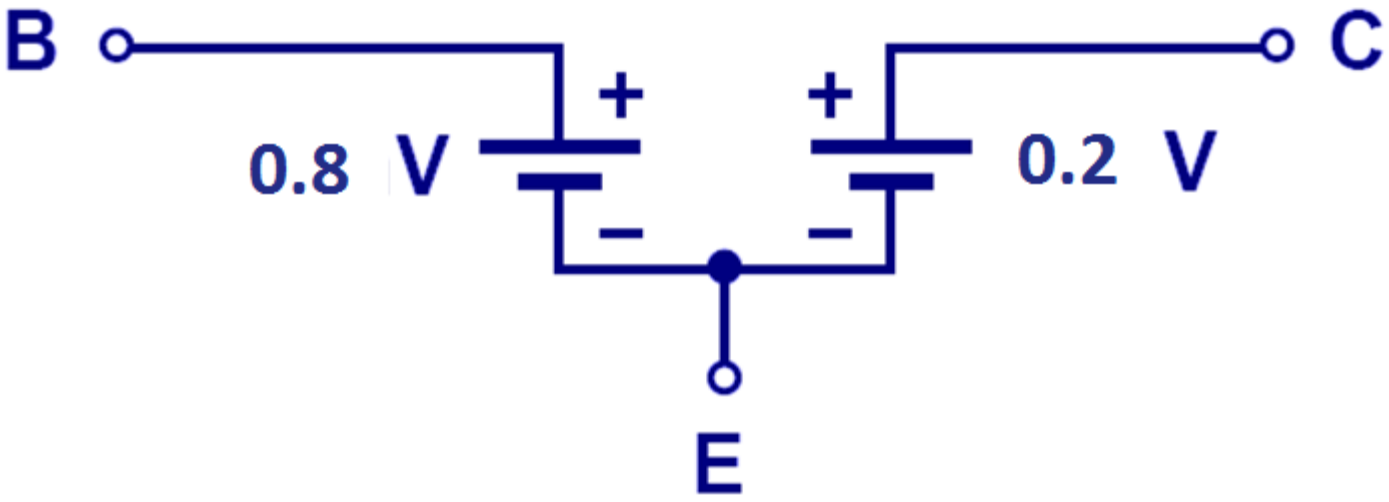


- When collector voltage drops below base voltage and forward biases the collector-base junction, base current increases and decreases the current gain factor, β.

Overall I/V Characteristics



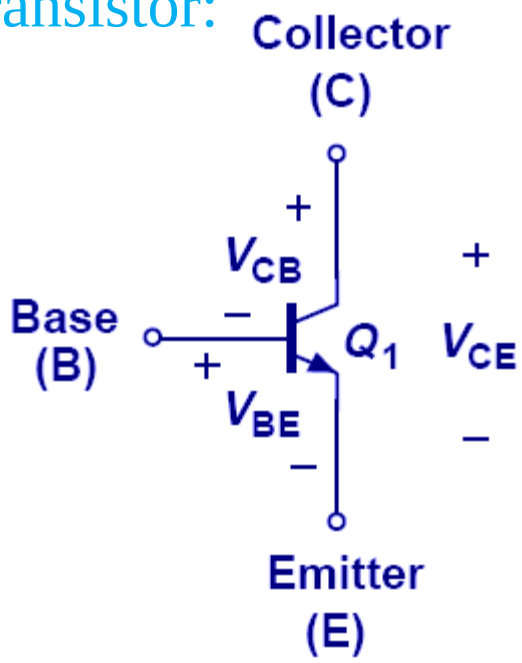
Deep Saturation



- In deep saturation region, the transistor loses its voltage-controlled current capability and V_{CE} becomes constant.

NPN Transistor: Active and Saturation Modes

NPN Transistor:



Active mode:

$V_{BE}=V_{BE\ ON}$ (~ 0.8 V)

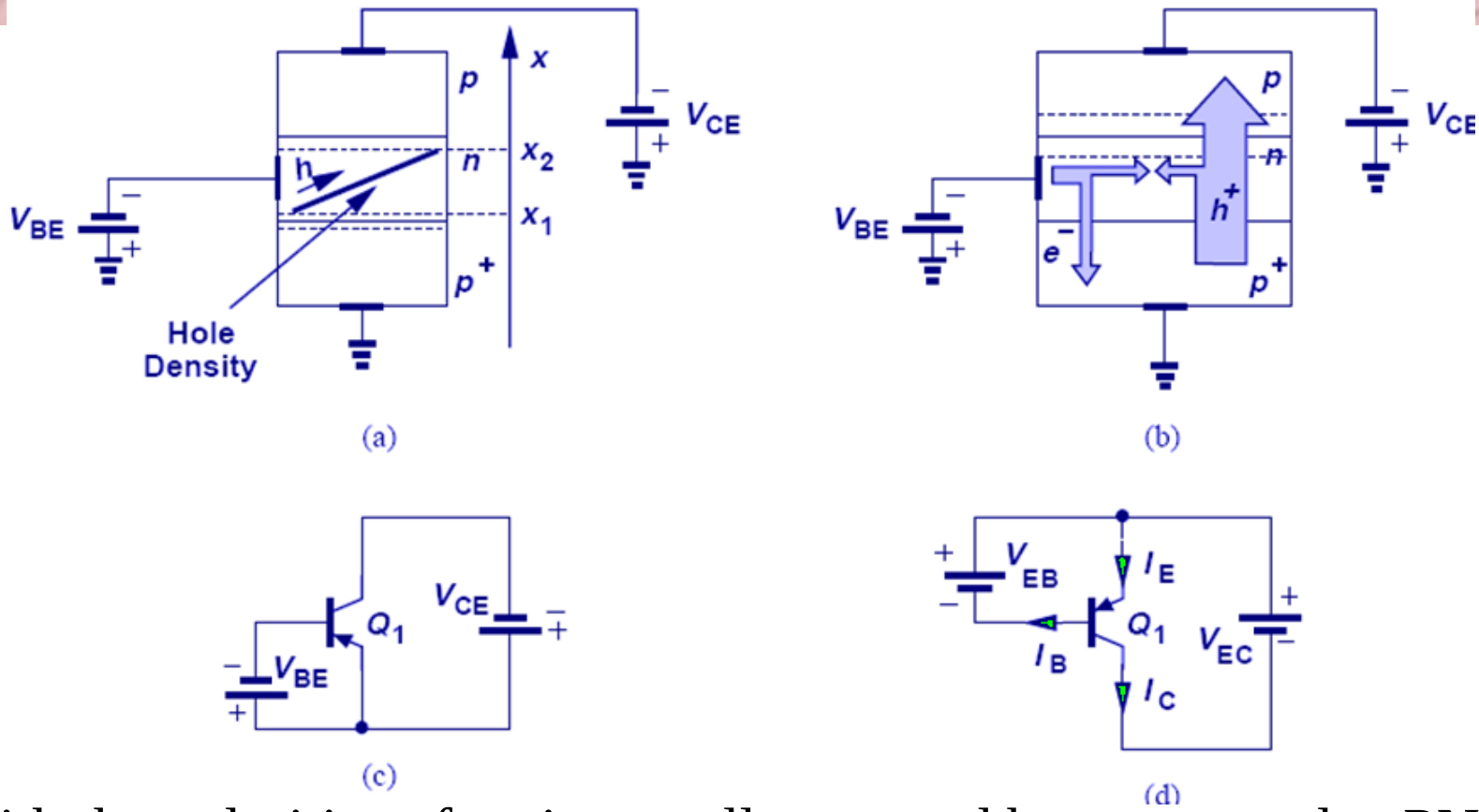
$V_{CE}>V_{CE\ sat}$ (~ 0.2 V)

Saturation mode:

$V_{BE}=V_{BE\ sat}$ (~ 0.8 V)

$V_{CE}=V_{CE\ sat}$ (~ 0.2 V)

PNP Transistor



- With the polarities of emitter, collector, and base reversed, a PNP transistor is formed.
- All the principles that applied to NPN's also apply to PNP's, with the exception that emitter is at a higher potential than base and base at a higher potential than collector.

PNP Equations

$$I_C = I_S \exp \frac{V_{EB}}{V_T}$$

$$I_B = \frac{I_S}{\beta} \exp \frac{V_{EB}}{V_T}$$

$$I_E = \frac{\beta + 1}{\beta} I_S \exp \frac{V_{EB}}{V_T}$$

Early Effect ⇒

$$I_C = \left(I_S \exp \frac{V_{EB}}{V_T} \right) \left(1 + \frac{V_{EC}}{V_A} \right)$$

Summary of Active and Saturation Modes

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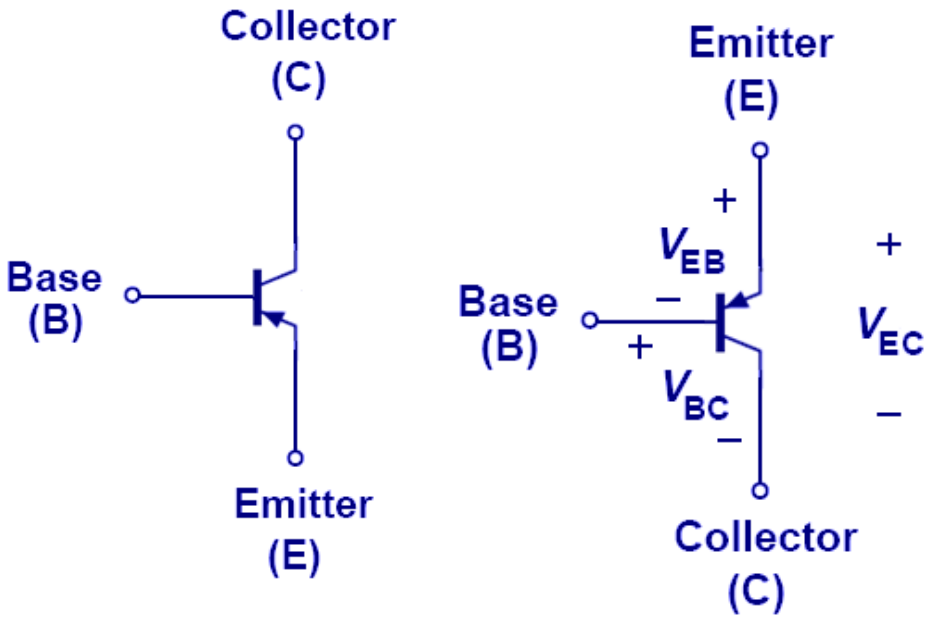
PNP Transistor:



Active mode:

$V_{EB}=V_{EB\ ON}$ (~ 0.8 V)

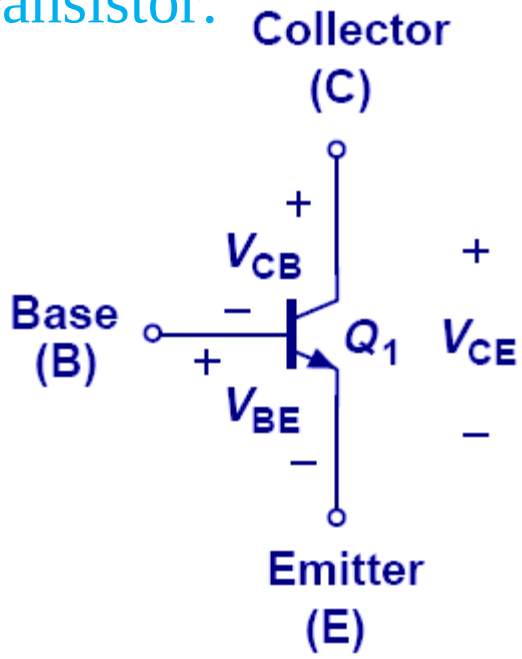
$V_{EC}>V_{EC\ sat}$ (~ 0.2 V)

Saturation mode:

$V_{EB}=V_{EB\ sat}$ (~ 0.8 V)

$V_{EC}=V_{EC\ sat}$ (~ 0.2 V)

NPN Transistor:



Active mode:

$V_{BE}=V_{BE\ ON}$ (~ 0.8 V)

$V_{CE}>V_{CE\ sat}$ (~ 0.2 V)

Saturation mode:

$V_{BE}=V_{BE\ sat}$ (~ 0.8 V)

$V_{CE}=V_{CE\ sat}$ (~ 0.2 V)

Bipolar DC Analysis

الکترونیک ۱

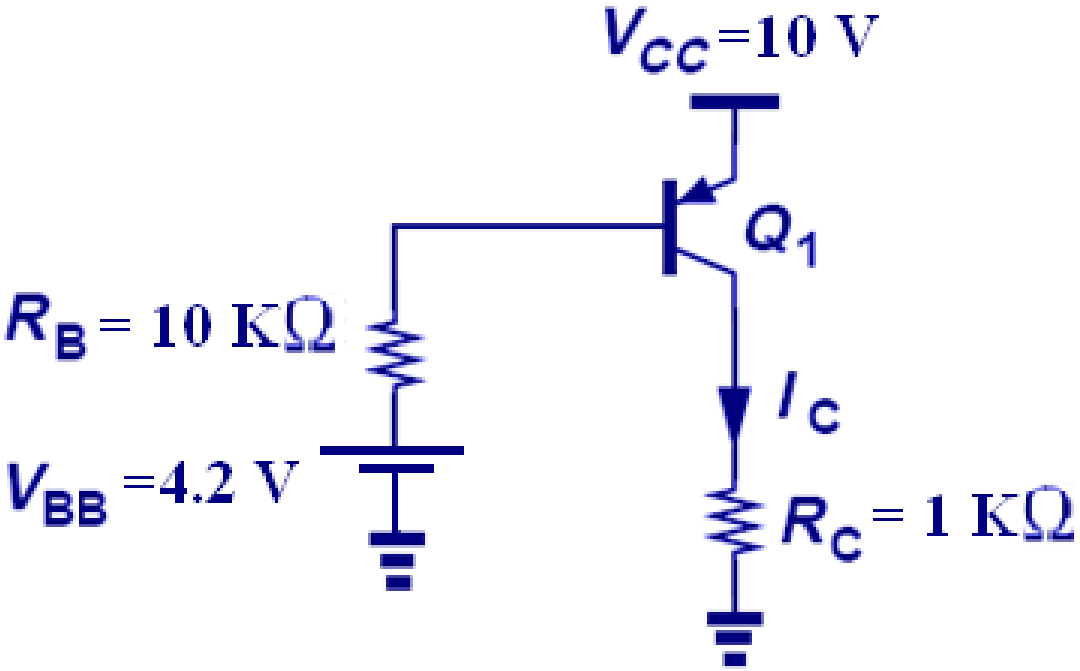
- "dc analysis" or "bias analysis" :
- this step determines:
  - The region of operation (active or saturation)
  - (I_E , I_C , I_B) and V_{CE}

$$Q\ \ point: \begin{cases} I_{C\ Q} \\ V_{CE\ Q} \end{cases}$$

Problem-Solving Technique: Bipolar DC Analysis

- 1. Assume that the transistor is biased in the forward-active mode in which case $V_{BE} = V_{BE\,(on),}\ I_B > 0$, and $I_C = \beta I_B$.
- 2. Analyze the "linear" circuit with this assumption.
- 3. Evaluate the resulting state of the transistor. If the initial assumption is "active mode" , and for NPN transistor $V_{CE} > V_{CE\ sat}$ is true(for PNP transistor, $V_{EC} > V_{EC\ sat}$), then the initial assumption is correct. However, if the calculation shows $I_B < 0$, then the transistor is probably "cut off", and if the calculation shows for NPN transistor $V_{CE} < V_{CE\,sat}$(for PNP transistor, $V_{EC} < V_{EC\ sat}$), the transistor is likely biased in "saturation".
- 4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed. Step 3 must then be repeated.

Example 1: PNP Transistor



- β=10
- $V_{EB\ ON}$=0.8 V
- $V_{EC\ sat}$=0.2 V

- I_C :?
- I_B :?
- V_{EC} :?

I_c=5 mA

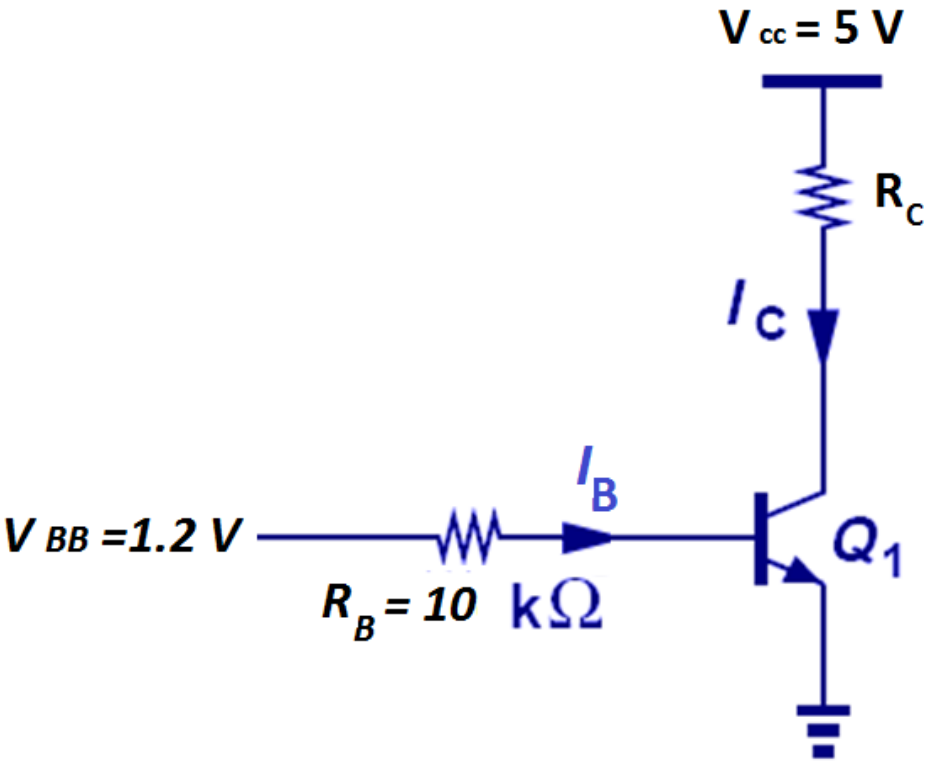
V_{EC}=5 V

- If R_C=3 KΩ ; I_C , I_B , V_{EC} :?

b) V_{EC}=0.2 V

b) I_c=3.3 mA

Example 2: NPN Transistor



- β=100
- R_C=0.5 KΩ
- $V_{BE\ ON}$=0.8 V
- $V_{CE\ sat}$=0.2 V

- I_C :?
- I_B :?
- V_{CE} :?

I_c=4 mA

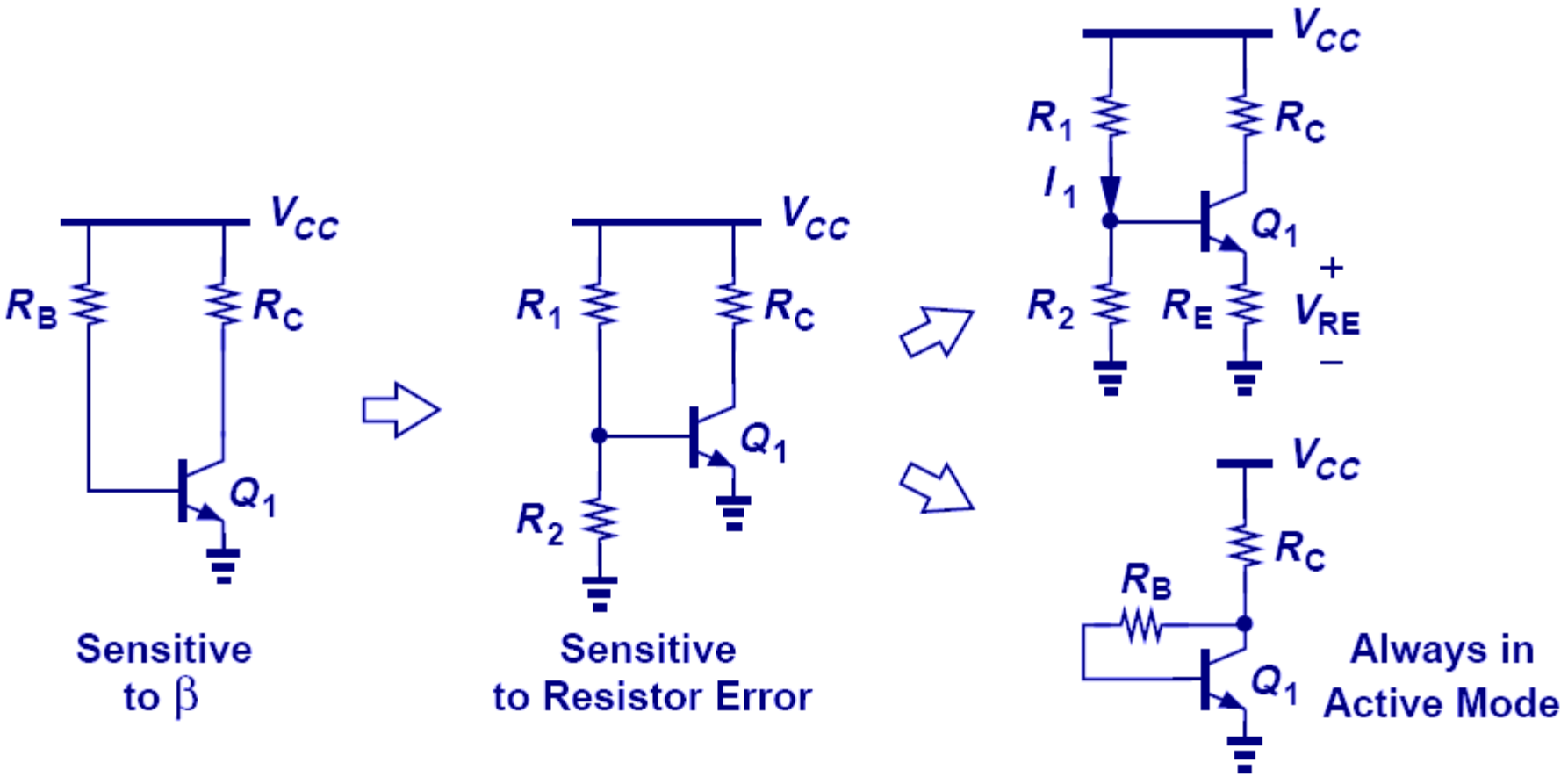
V_{CE}=3 V

- If R_C=2 KΩ ; I_C , I_B ,V_{CE} :?

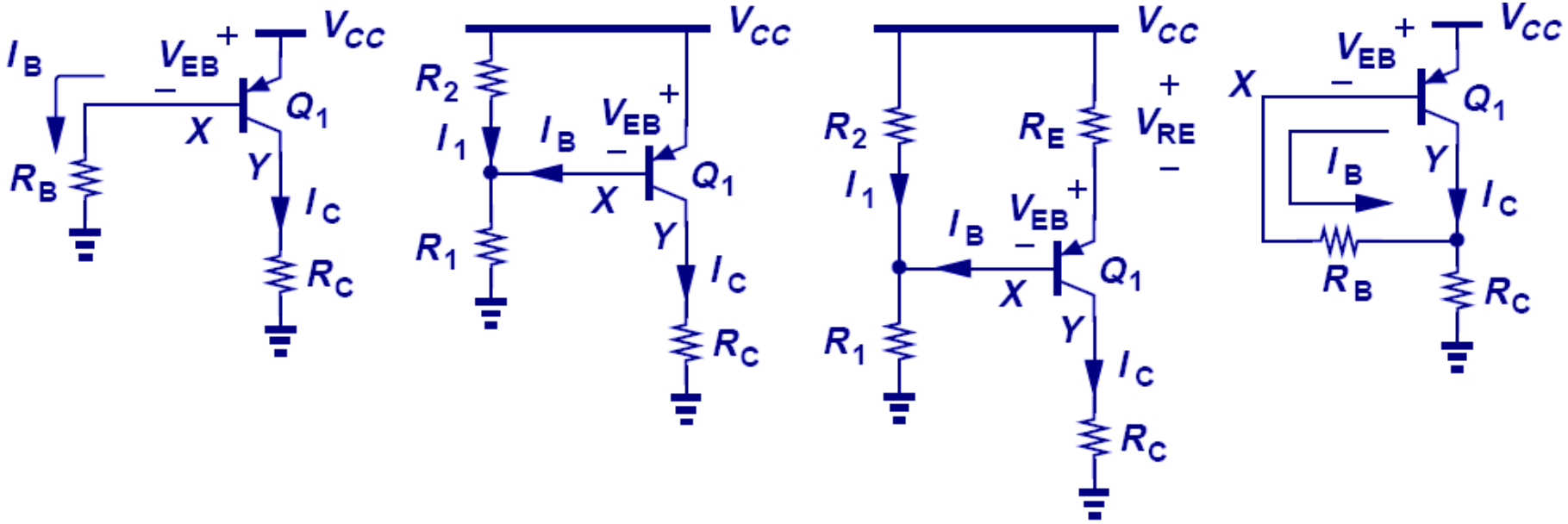
b) V_{CE}=0.2 V

b) I_c=2.4 mA

Summary of Biasing Techniques

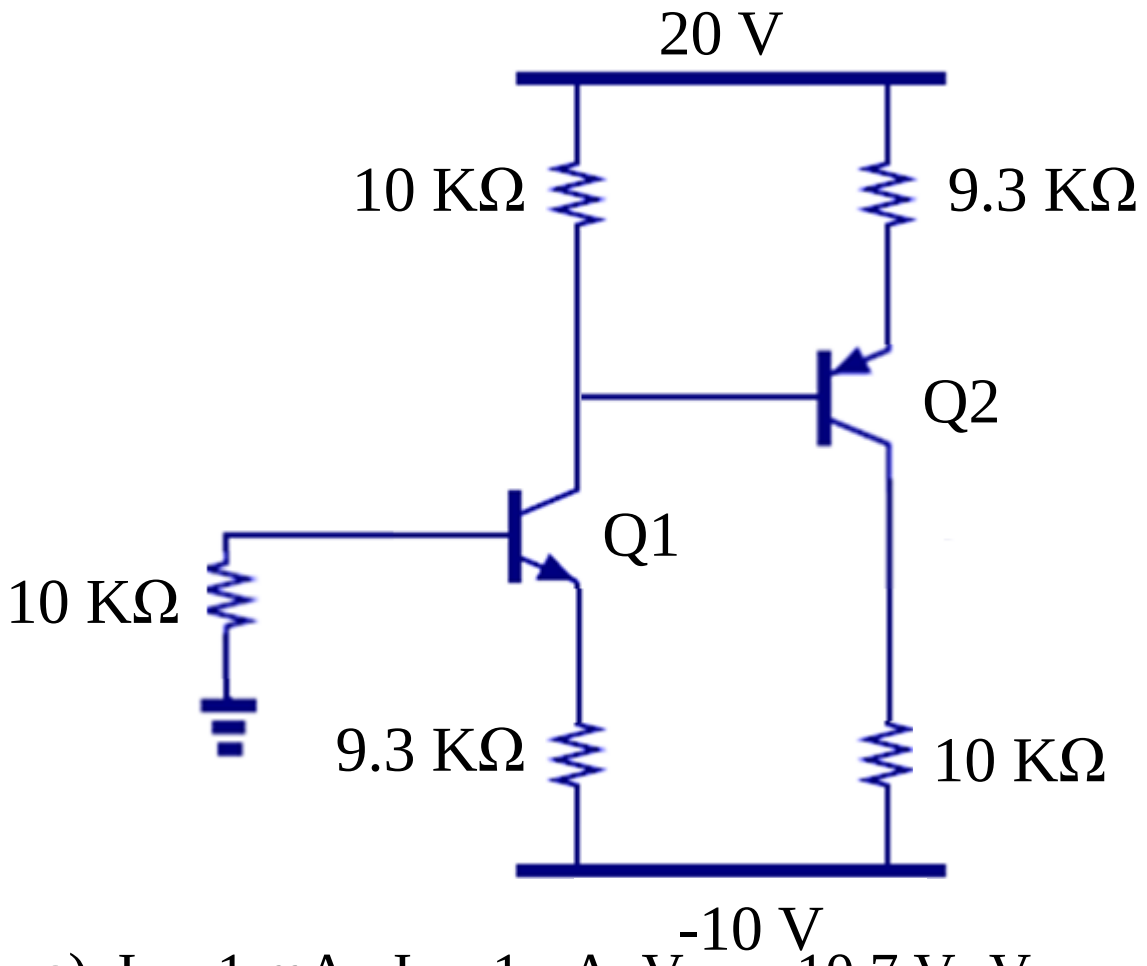


PNP Biasing Techniques



- Same principles that apply to NPN biasing also apply to PNP biasing with only polarity modifications.

Example: 2 Stage Transistor



- $\beta \rightarrow \infty$
- $V_{BE\ ON}=0.7$ V
- $V_{CE\ sat}=0.2$ V
- $I_{C1}, I_{C2}=?$

- If $\beta=100$:
- $I_{C1}, I_{C2}=?$

a) $I_{c1}=1$ mA, $I_{c\,2}=1$ µA, $V_{CE\,1}=10.7$ V$=V_{CE\,2}$

b) $I_{c1}=0.98$ mA, $I_{b1}=9.8$ µA, $I_{e1}=0.99$ mA

b) $I_{c1}=0.96$ mA, $I_{b1}=9.6$ µA, $I_{e1}=0.97$ mA

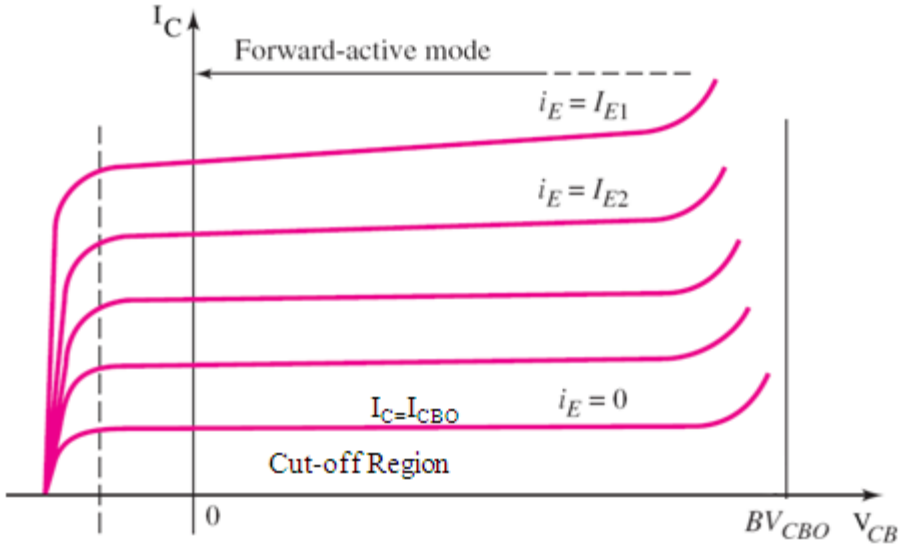
Cutoff Region

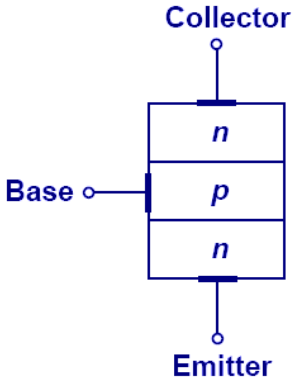
- Cutoff represents the off mode in switching applications. :open switch (one of the two states requires for binary logic circuits.)

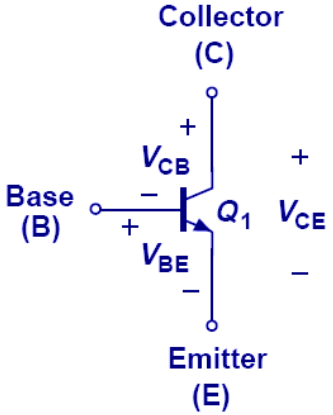
$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

Base-Emitter	Collector-Base	Transistor Mode
FB	RB	Forward active
FB	FB	Saturation
RB	RB	Cutoff







- For Silicon transistor and around room temperature we have:

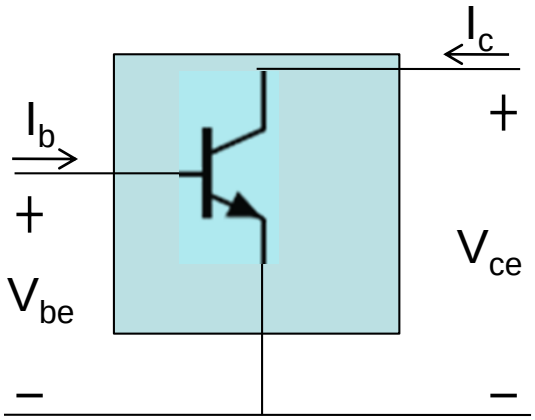
$$I_{CBO(T2)} \approx I_{CBO(T1)} \times 2^{\Delta T/10}$$

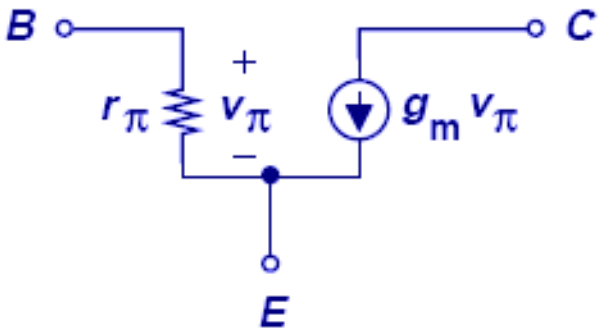
Course Overview

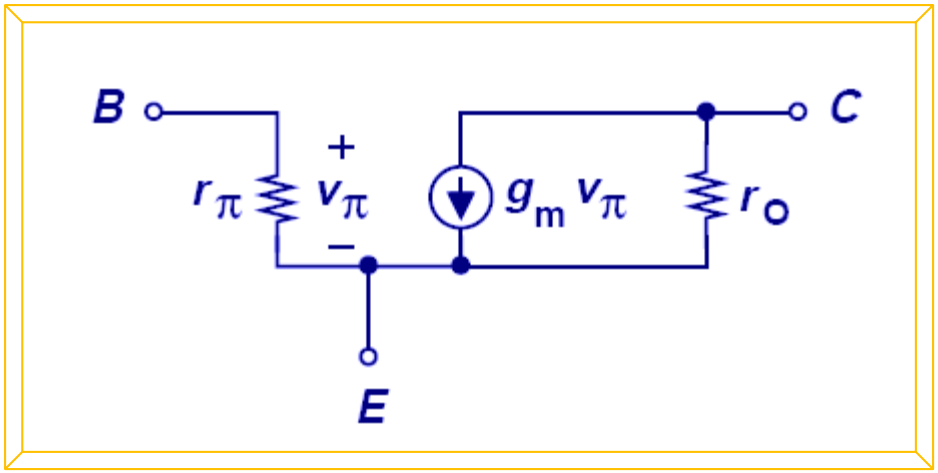
الکترونیک ۱

- Semiconductor physics
- PN junction
- BJT
  - BJT physics
  - dc analysis
- **BJT : Small signal analysis**
- Amplifiers
- MOSFET

Small-Signal Model

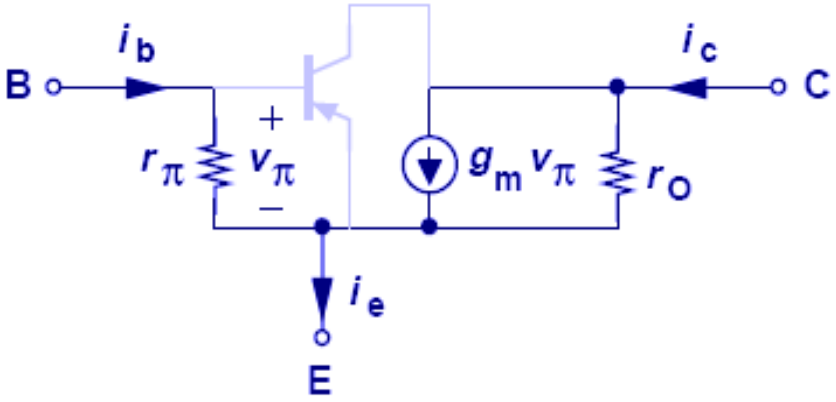




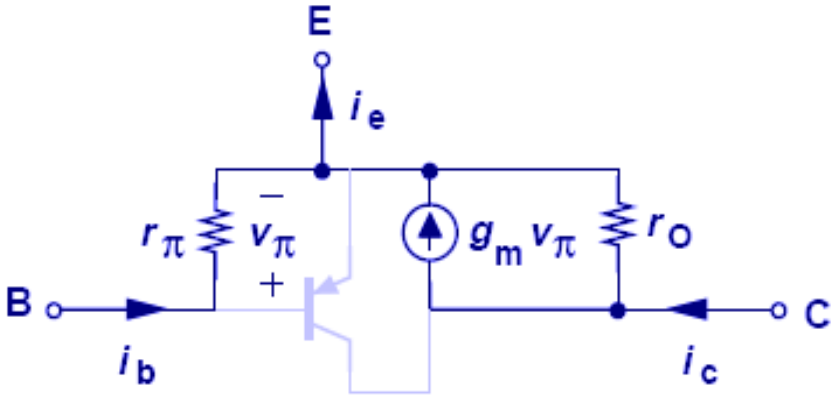


Small-Signal Model of BJT
(Hybrid π Model)

Small-Signal Model for PNP Transistor



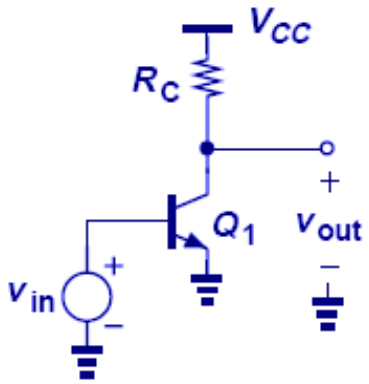
(a)

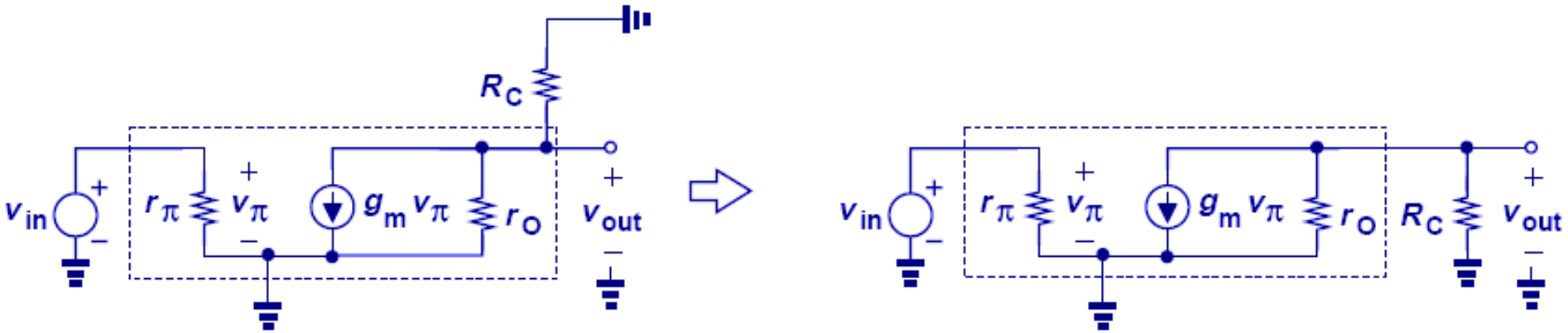


(b)

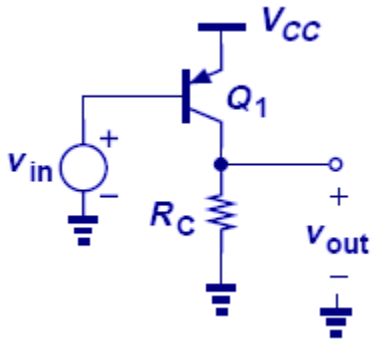
- The small signal model for PNP transistor is exactly IDENTICAL to that of NPN. This is not a mistake because the current direction is taken care of by the polarity of V_{BE}.

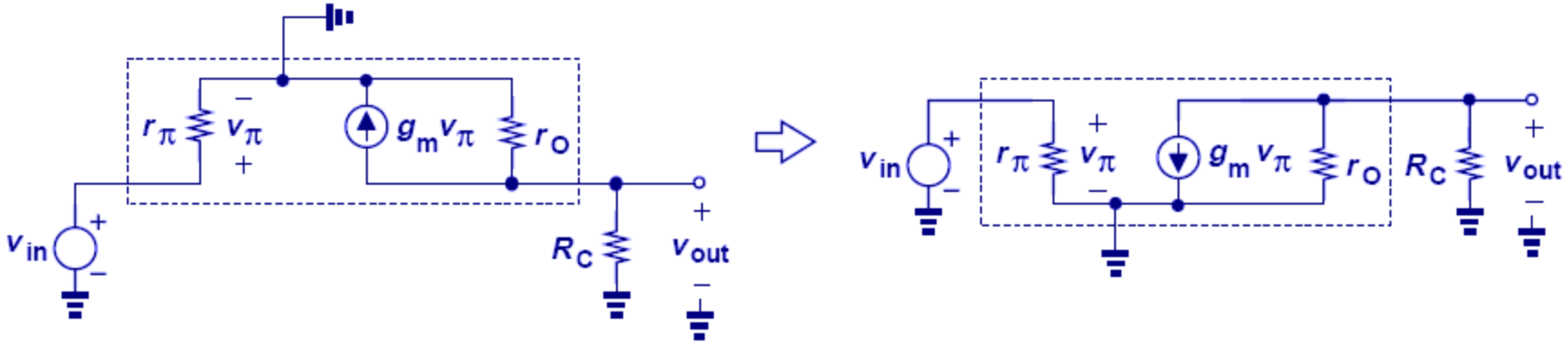
Small Signal Model Example I





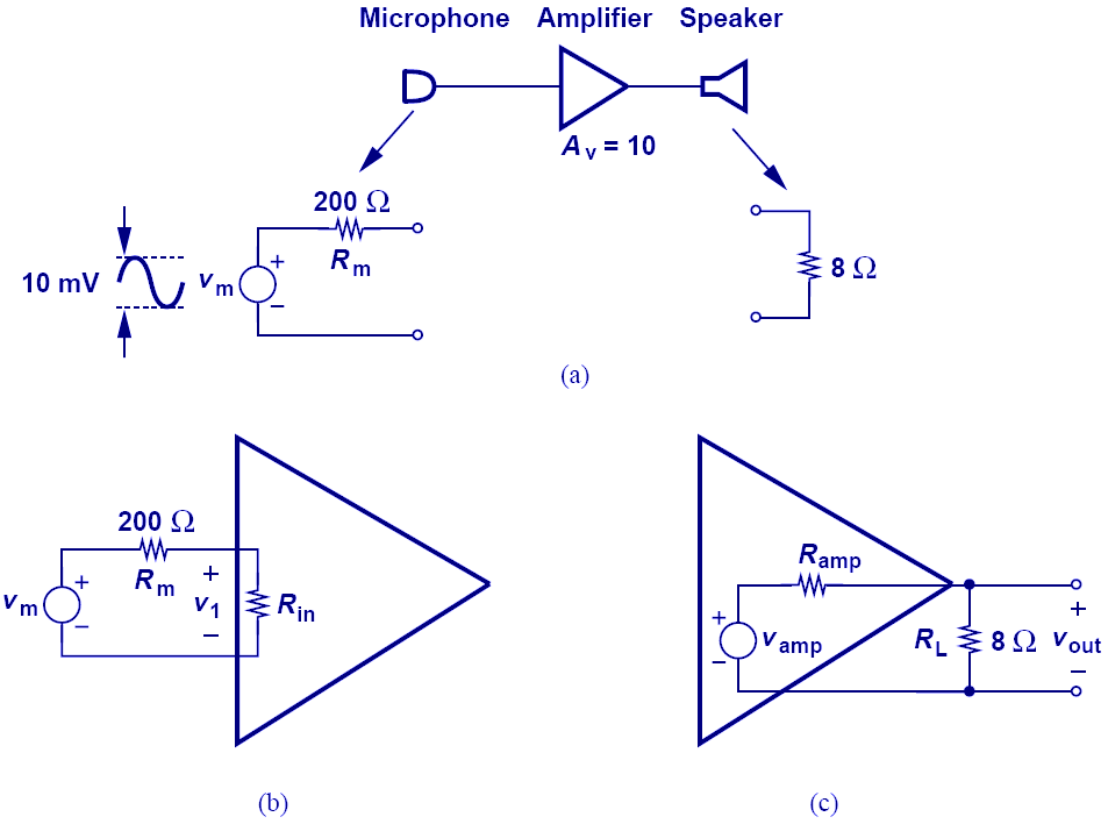
Small Signal Model Example II





- Small-signal model is identical to the previous ones.

Voltage Amplifier



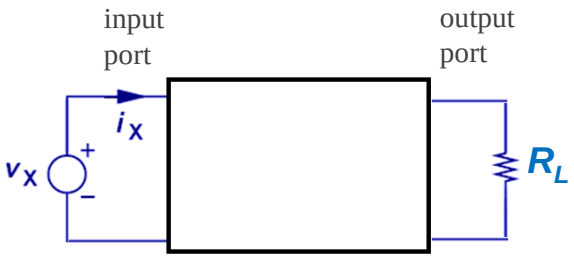
- Input (output) impedance is measured between the input (output) nodes of the circuit while all independent sources in the circuit are set to zero.

- In an ideal voltage amplifier, the input impedance is infinite and the output impedance zero.
- But in reality, input or output impedances depart from their ideal values.

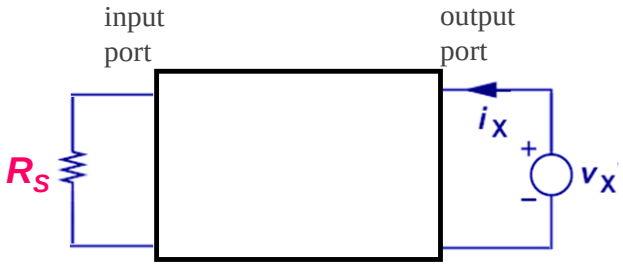
Input/Output Resistance

- What is the input and output resistance for this circuit?

- Definition of **input resistance:** $\mathbf{R_{in}}=v_x/i_x$

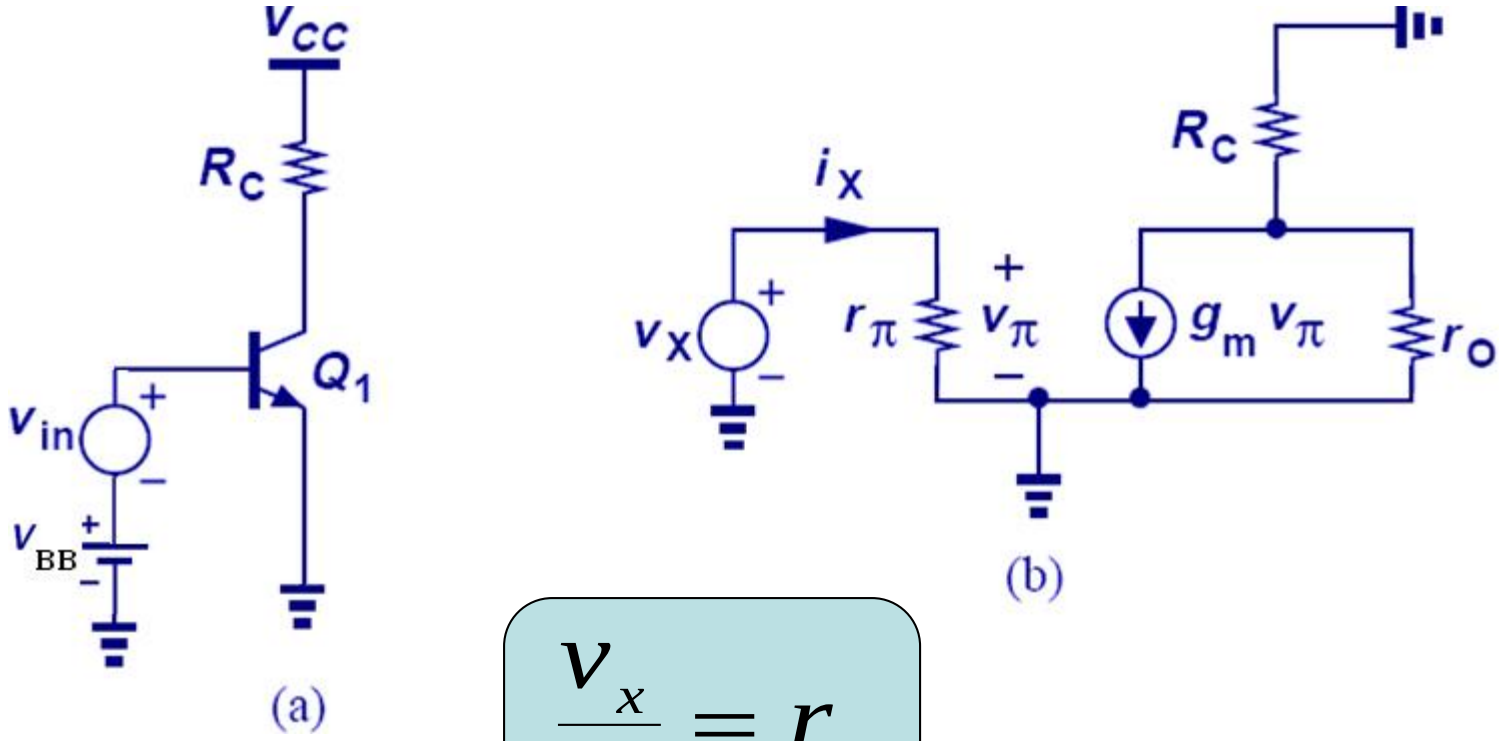


- Definition of **output resistance:** $\mathbf{R_{out}}=v_x/i_x$

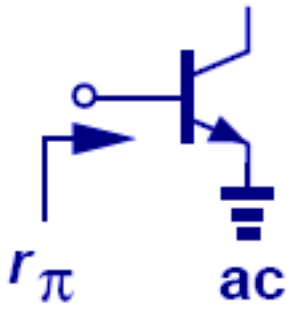


$$R_x = \frac{V_x}{i_x}$$

Input Impedance Example I

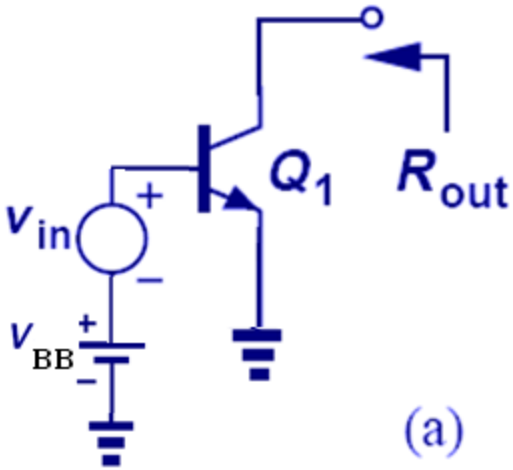


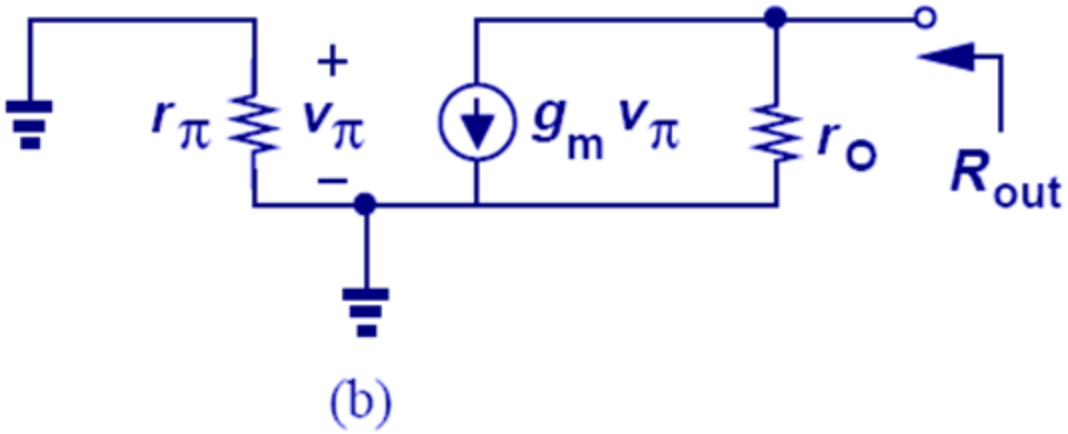
$$\frac{v_x}{i_x} = r_\pi$$



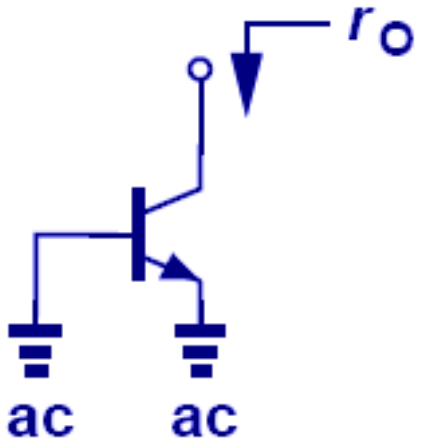
- When calculating input/output impedance, small-signal analysis is assumed.

Impedance at Collector



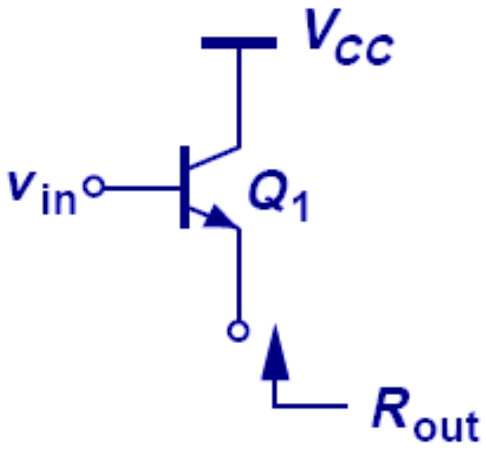


$$R_{out} = r_o$$

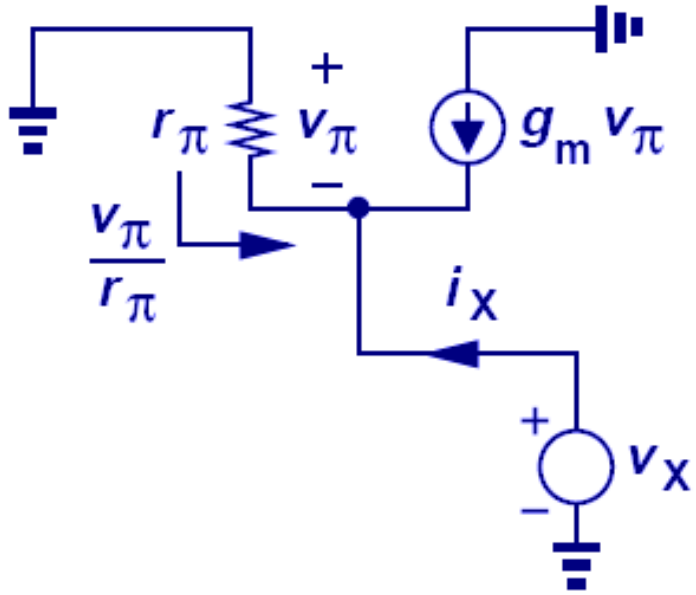


- With Early effect, the impedance seen at the collector is equal to the intrinsic output impedance of the transistor (if emitter is grounded).

Impedance at Emitter



(a)



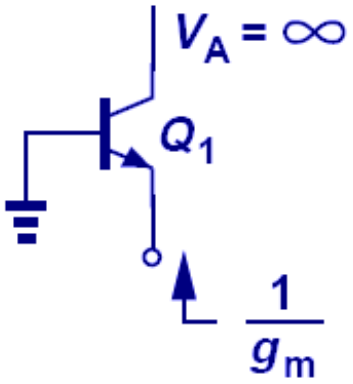
(b)

$$\frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{r_\pi}}$$

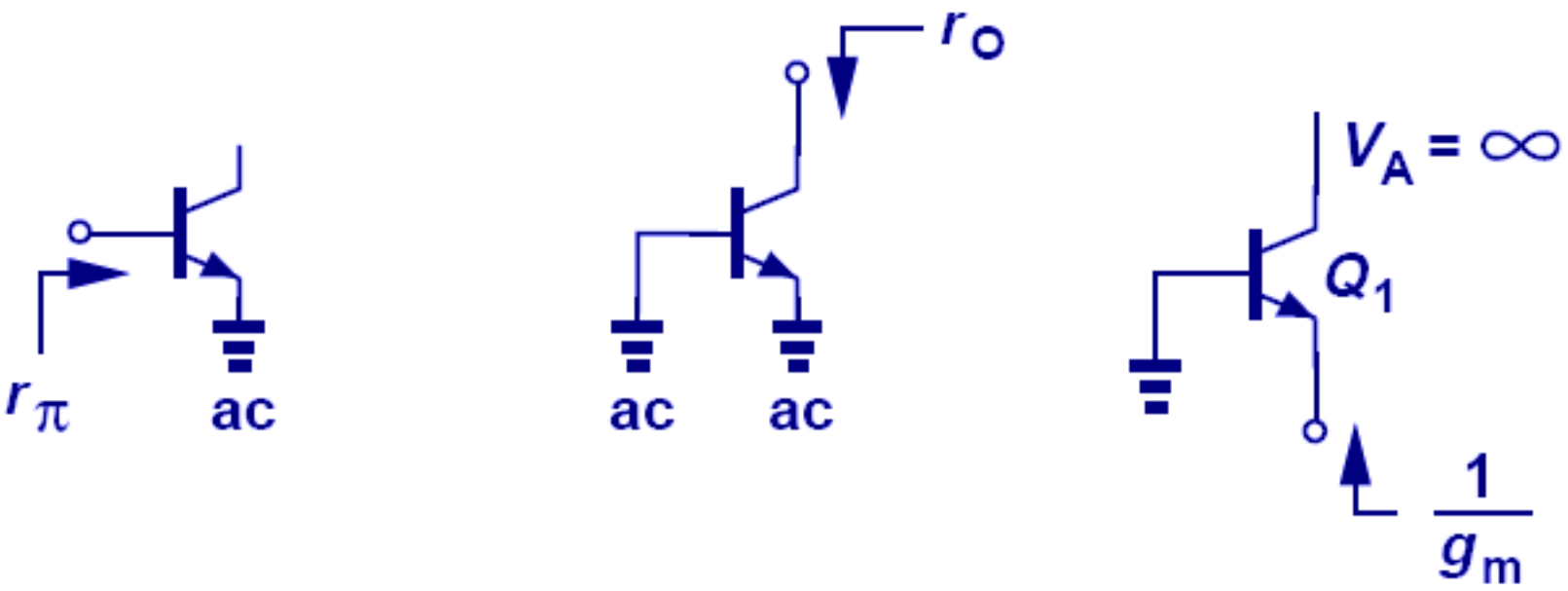
$$R_{out} \approx \frac{1}{g_m}$$

$$(V_A = \infty)$$

- The impedance seen at the emitter of a transistor is approximately equal to one over its transconductance (if the base is grounded).

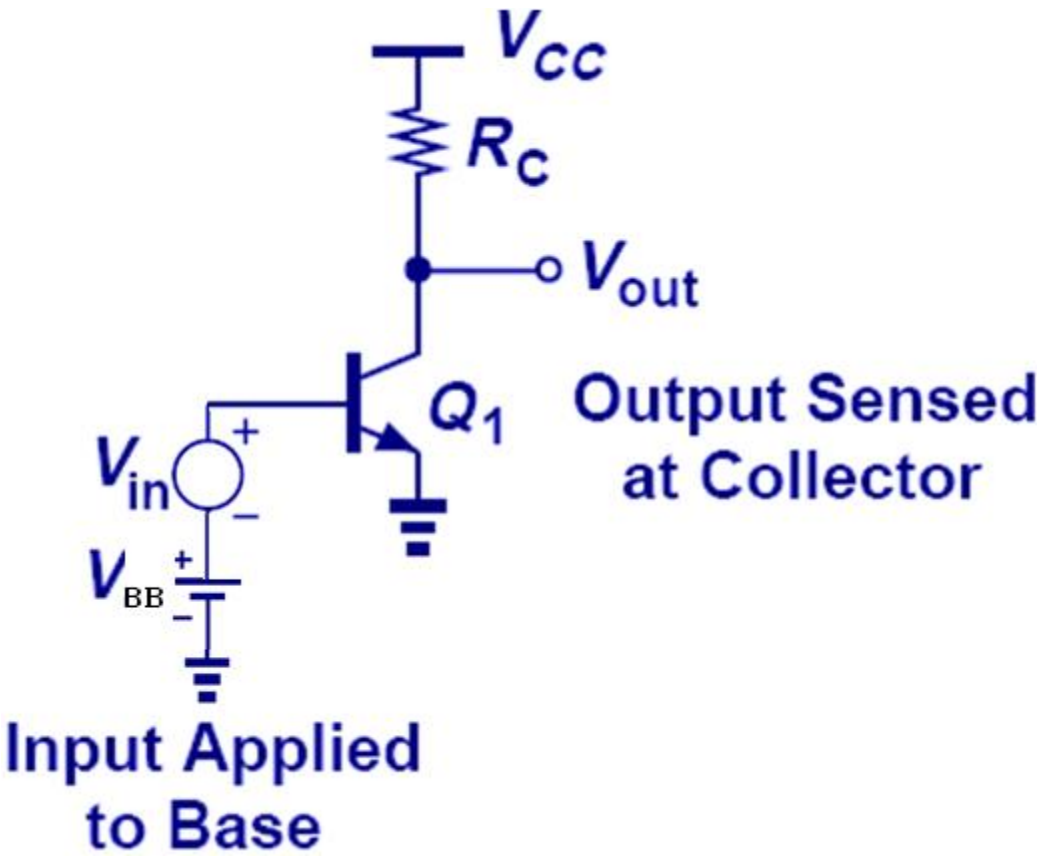


Three Master Rules of Transistor Impedances

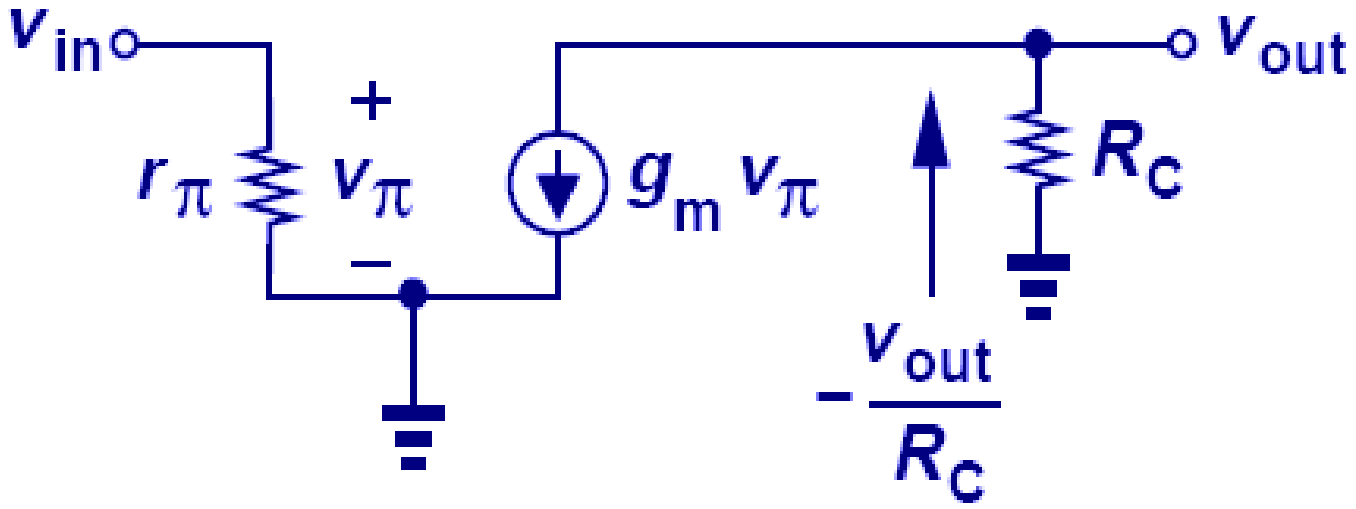


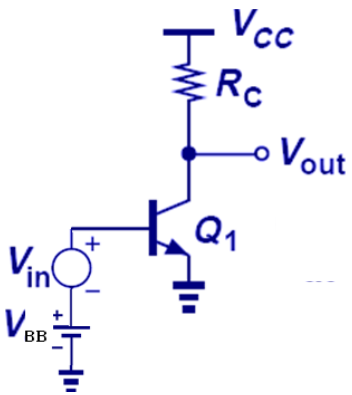
- Rule # 1: looking into the base, the impedance is r_π if emitter is (ac) grounded.
- Rule # 2: looking into the collector, the impedance is r_o if emitter is (ac) grounded.
- Rule # 3: looking into the emitter, the impedance is $1/g_m$ if base is (ac) grounded and Early effect is neglected.

Common-Emitter Topology



Small Signal of CE Amplifier



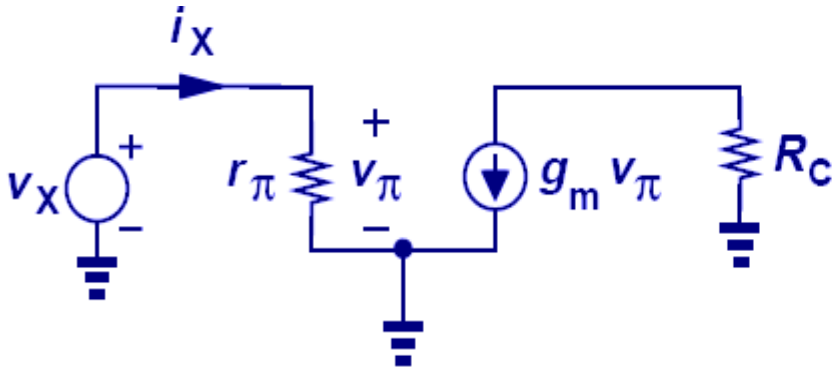


$$A_v = \frac{v_{out}}{v_{in}}$$

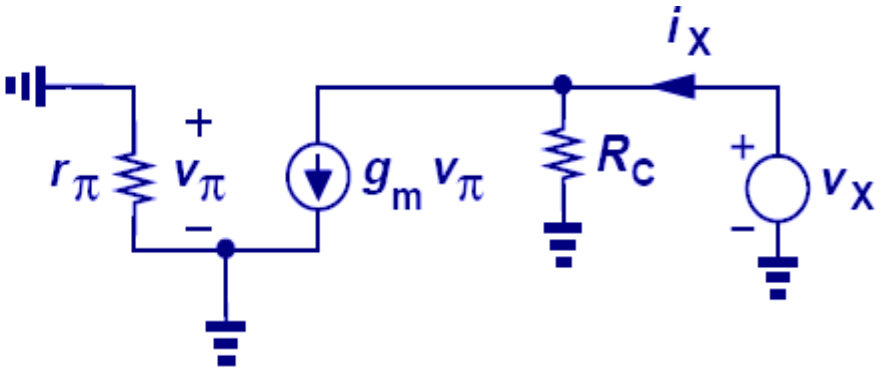
$$-\frac{v_{out}}{R_C} = g_m v_\pi = g_m v_{in}$$

$$A_v = -g_m R_C$$

I/O Impedances of CE Stage



(a)



(b)

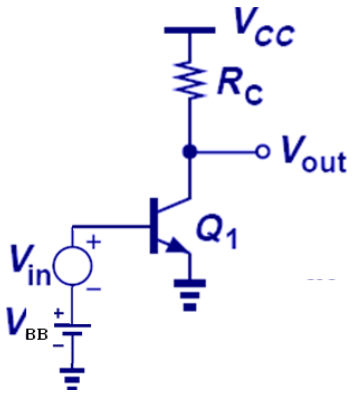
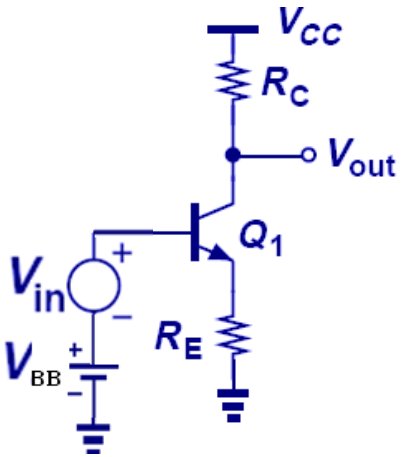
$$R_{in} = \frac{v_X}{i_X} = r_\pi$$

$$R_{out} = \frac{v_X}{i_X} = R_C$$

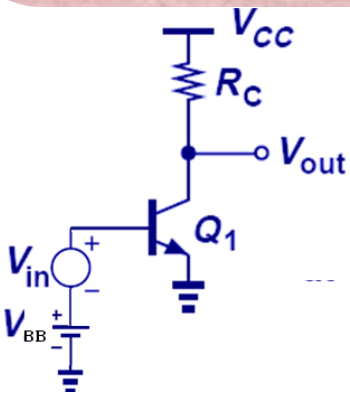
- When measuring output impedance, the input port has to be grounded so that $V_{in} = 0$.

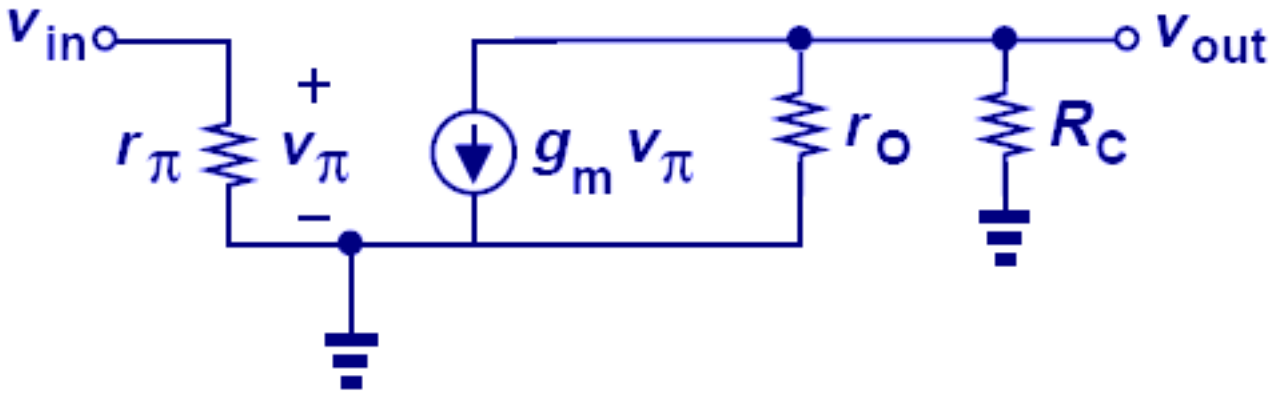
Small Signal of CE Amplifier

الکترونیک ۱

	Without Early effect	With Early effect
	$A_v = -g_m R_C$ $R_{in} = r_\pi$ $R_{out} = R_C$	
		

Inclusion of Early Effect





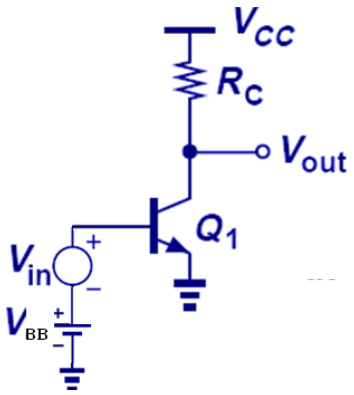
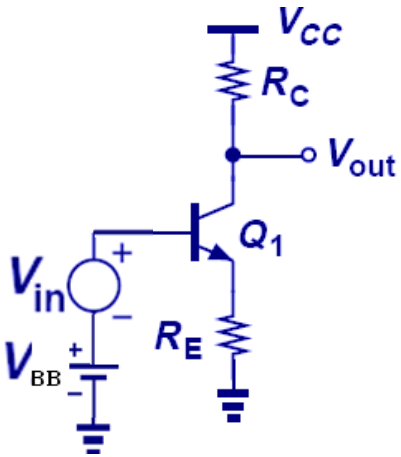
$$A_v = -g_m (R_C \| r_O)$$

$$R_{out} = R_C \| r_O$$

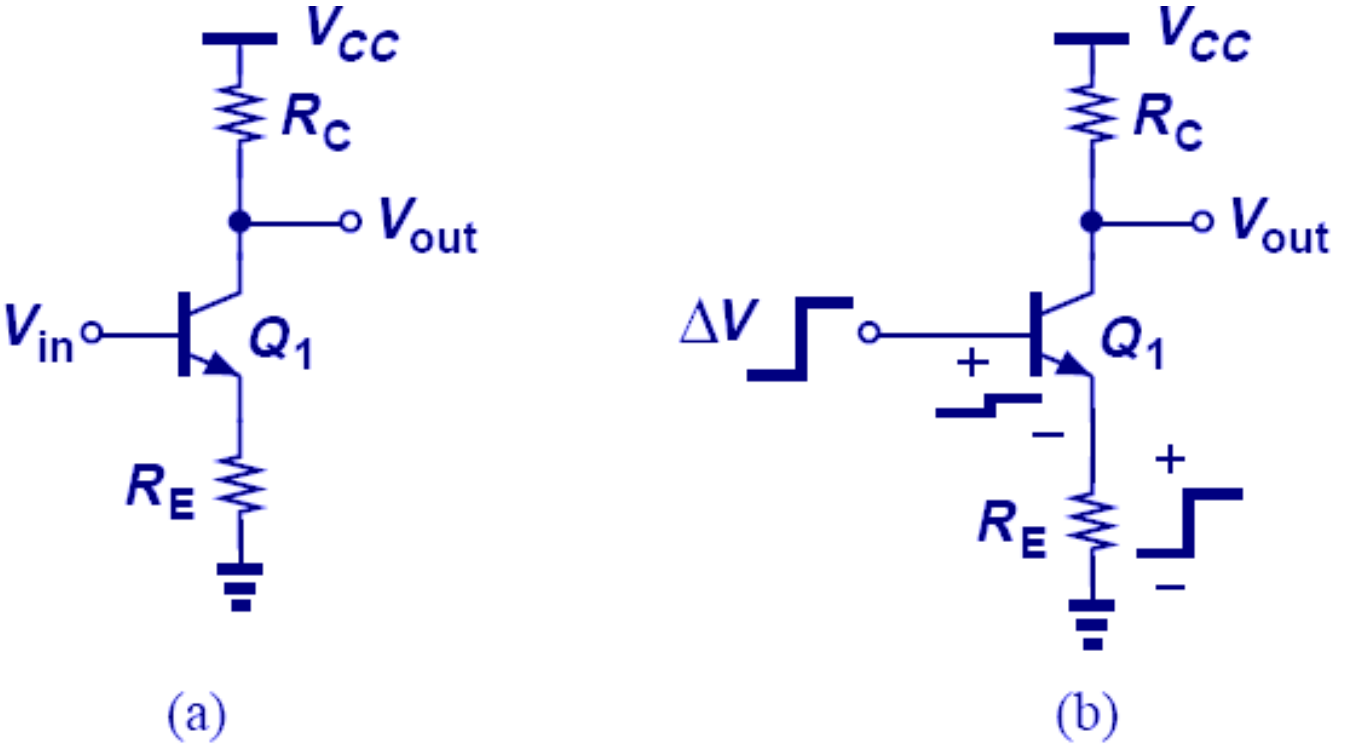
- Early effect will lower the gain of the CE amplifier, as it appears in parallel with R_C.

Small Signal of CE Amplifier

الکترونیک ۱

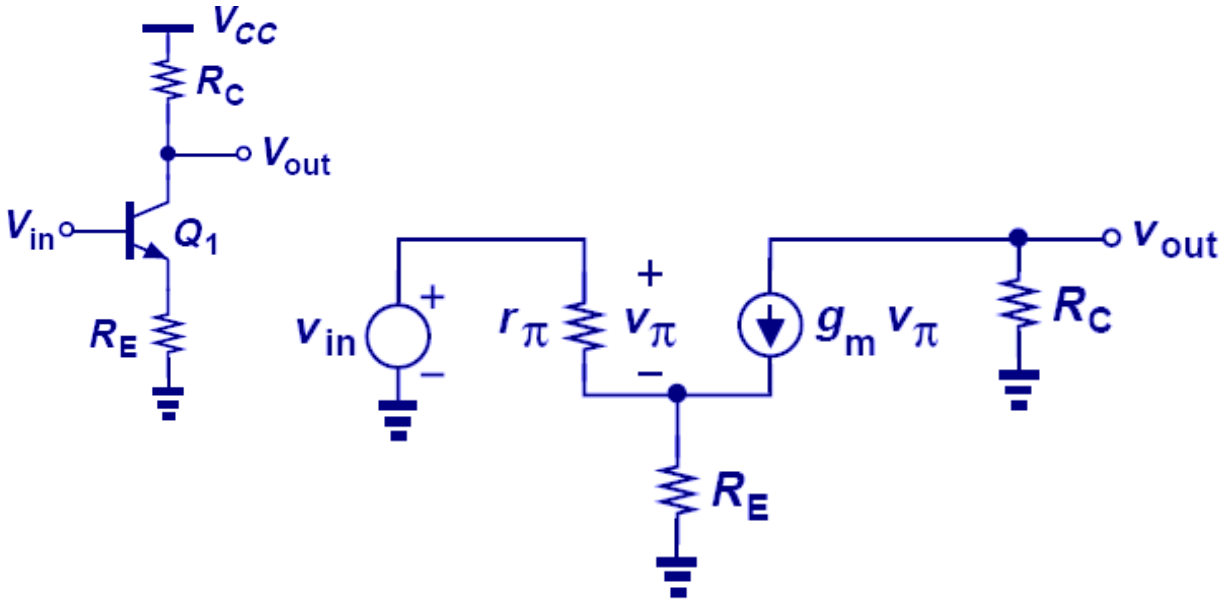
	Without Early effect	With Early effect
	$A_v = -g_m R_C$ $R_{in} = r_\pi$ $R_{out} = R_C$	$A_v = -g_m (R_C \parallel r_O)$ $R_{in} = r_\pi$ $R_{out} = R_C \parallel r_O$
		

Emitter Degeneration



- By inserting a resistor in series with the emitter, we "degenerate" the CE stage.
- This topology will decrease the gain of the amplifier but improve other aspects, such as linearity, and input impedance.

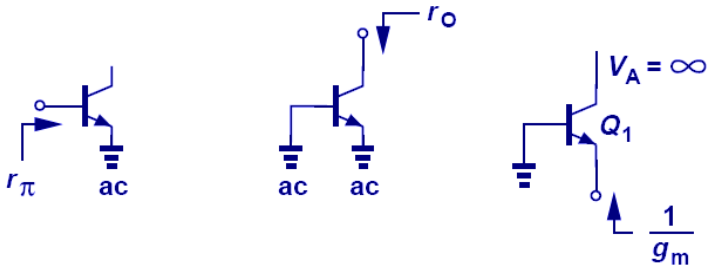
Emitter Degeneration



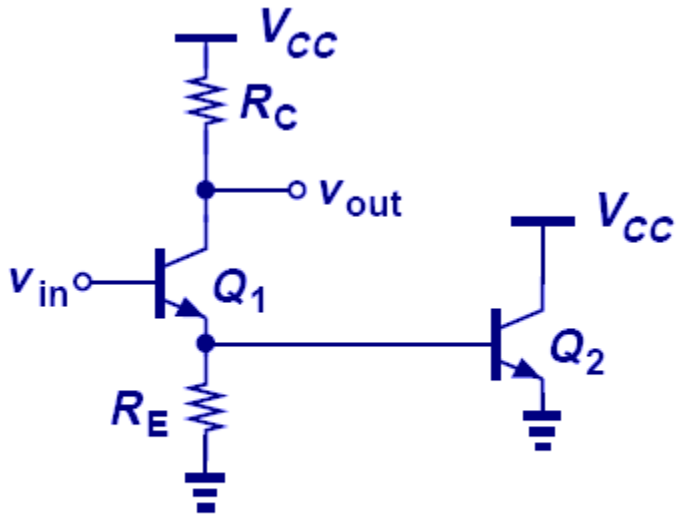
$$A_v = -\frac{g_m R_C}{1 + g_m R_E}$$

$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

- Interestingly, this gain is equal to the total load resistance to ground divided by $1/g_m$ plus the total resistance placed in series with the emitter.



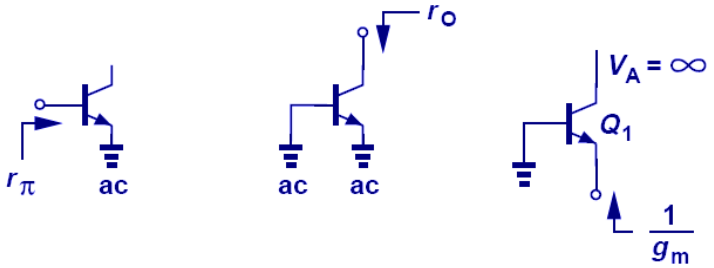
Emitter Degeneration Example



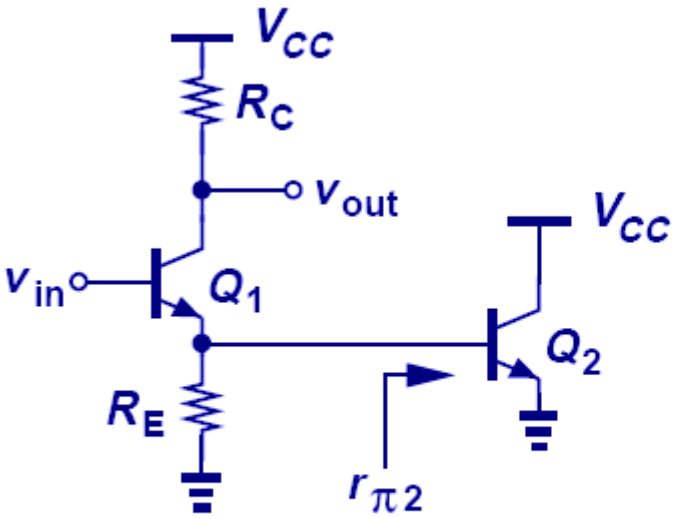
(a)

$$A_v = ?$$

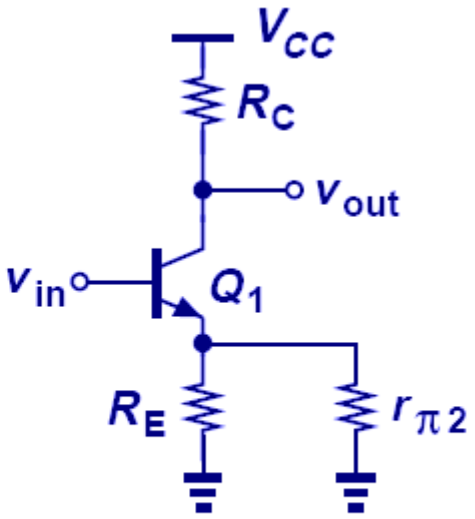
- The input impedance of Q_2 can be combined in parallel with R_E to yield an equivalent impedance that degenerates Q_1.



Emitter Degeneration Example



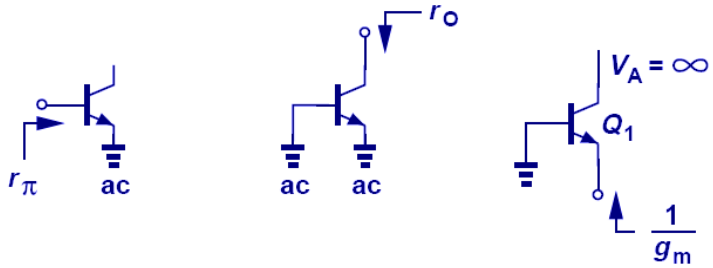
(a)



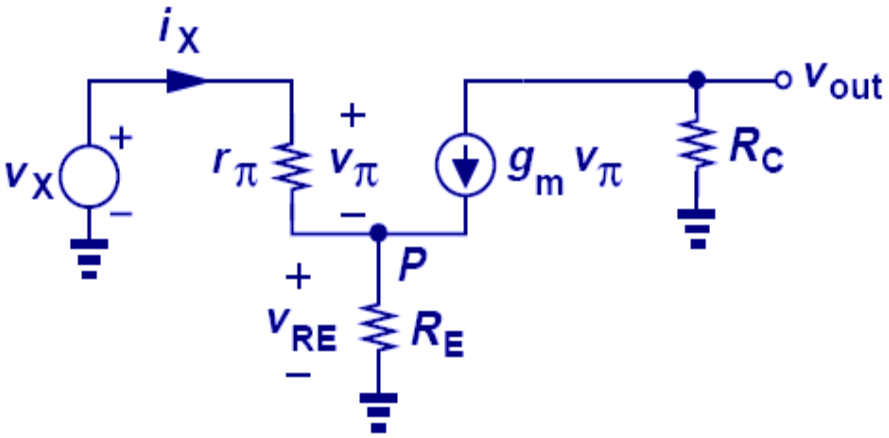
(b)

$$A_v = -\frac{R_C}{\frac{1}{g_{m1}} + R_E \| r_{\pi 2}}$$

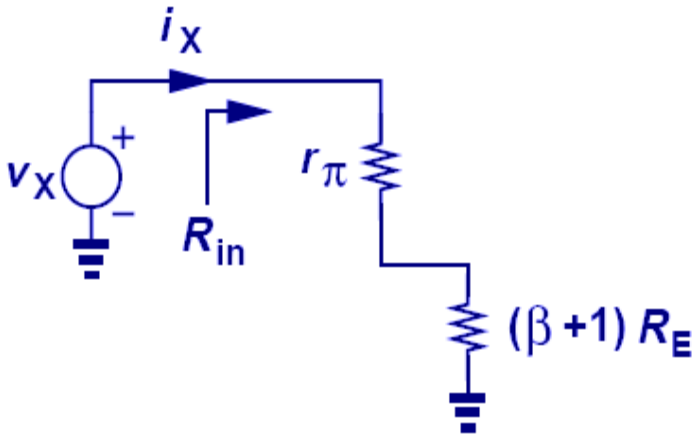
- The input impedance of Q_2 can be combined in parallel with R_E to yield an equivalent impedance that degenerates Q_1.



Input Impedance of Degenerated CE Stage



(a)



(b)

$$V_A = \infty$$

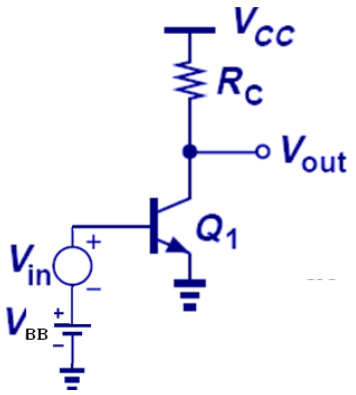
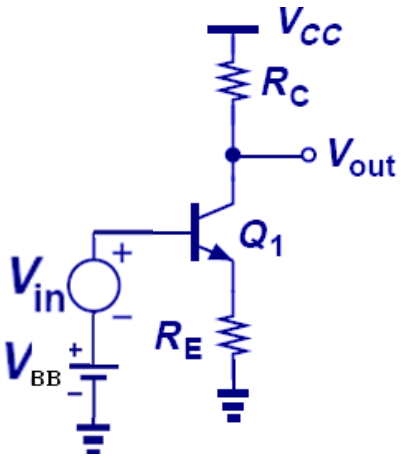
$$v_X = r_\pi i_X + R_E(1+\beta)i_X$$

$$R_{in} = \frac{v_X}{i_X} = r_\pi + (\beta+1)R_E$$

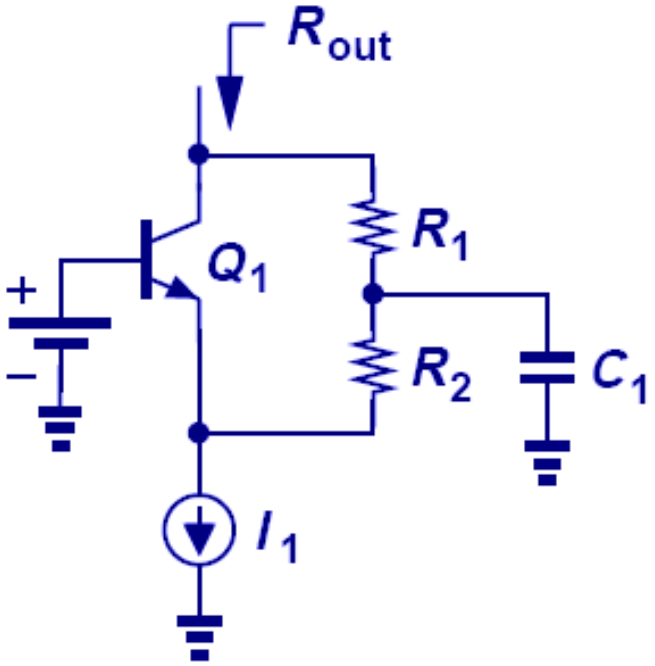
- With emitter degeneration, the input impedance is increased from r_π to $r_\pi + (\beta+1)R_E$; a desirable effect.

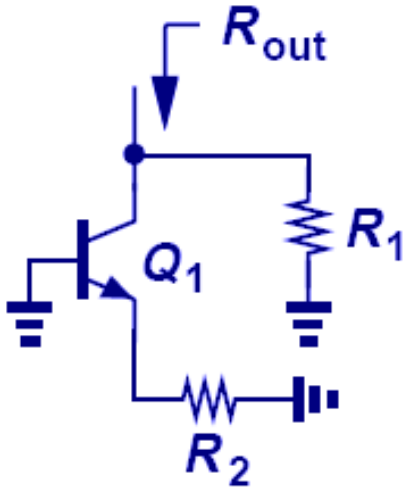
Small Signal of CE Amplifier

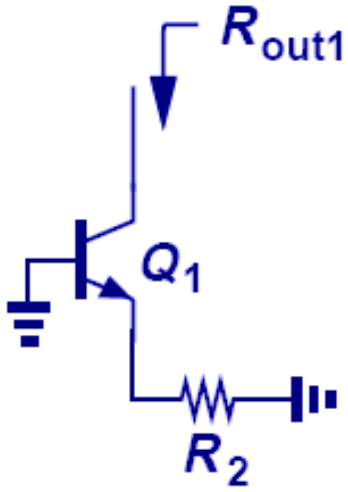
الکترونیک ۱

	Without Early effect	With Early effect
	$A_v = -g_m R_C$ $R_{in} = r_\pi$ $R_{out} = R_C$	$A_v = -g_m (R_C \parallel r_O)$ $R_{in} = r_\pi$ $R_{out} = R_C \parallel r_O$
	$A_v = -\dfrac{R_C}{\dfrac{1}{g_m} + R_E}$ $R_{in} = r_\pi + (\beta+1)R_E$ $R_{out} = R_C$	$A_v \approx -\dfrac{R_C}{\dfrac{1}{g_m} + R_E}$ $R_{in} \approx r_\pi + (\beta+1)R_E$ $R_{out} \approx (r_O[1 + g_m(R_E \parallel r_\pi)]) \parallel R_C$

Analysis by Inspection



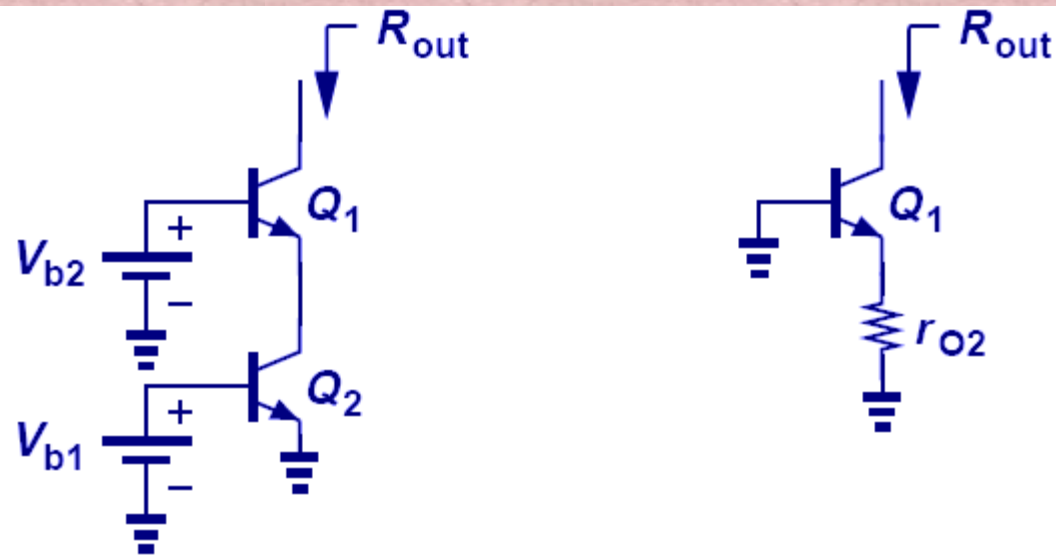




$$R_{out} = R_1 \parallel R_{out1} \Longrightarrow R_{out1} = [1 + g_m (R_2 \parallel r_\pi)] r_O \Longrightarrow R_{out} = [1 + g_m (R_2 \parallel r_\pi)] r_O \parallel R_1$$

- This seemingly complicated circuit can be greatly simplified by first recognizing that the capacitor creates an AC short to ground, and gradually transforming the circuit to a known topology.

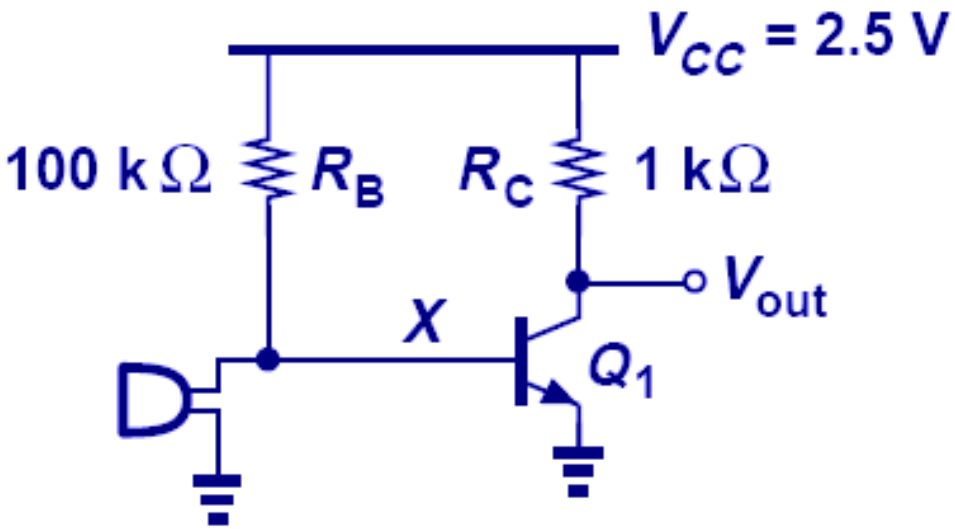
Example: Degeneration by Another Transistor



$$R_{out} = [1 + g_{m1}(r_{O2} \| r_{\pi 1})]r_{O1}$$

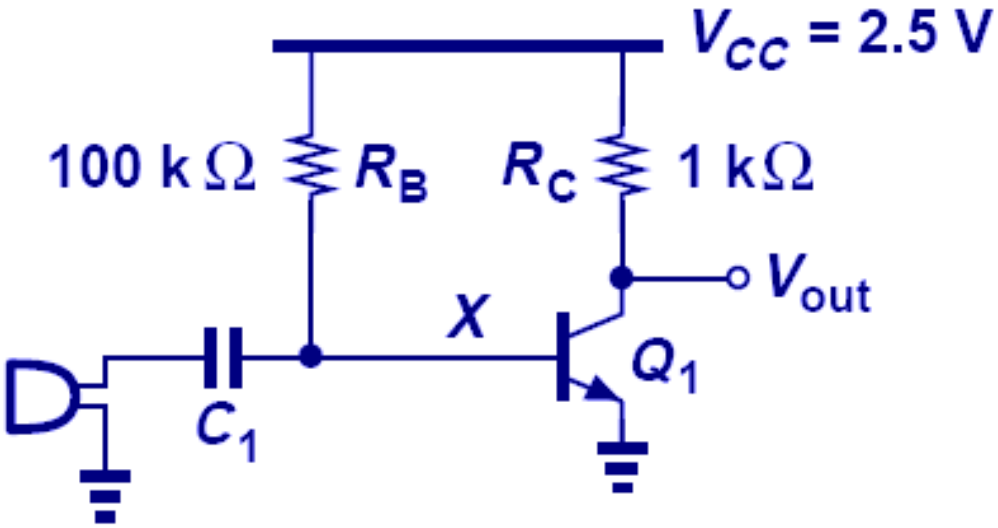
- Called a “cascode”, the circuit offers many advantages..

Bad Input Connection



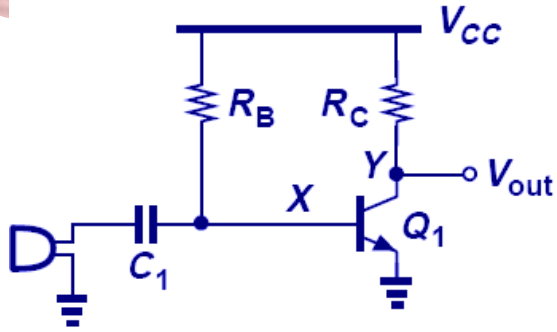
- Since the microphone has a very low resistance that connects from the base of Q_1 to ground, it attenuates the base voltage and renders Q_1 without a bias current.

Use of Coupling Capacitor

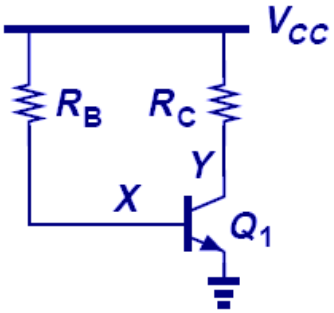


- Capacitor isolates the bias network from the microphone at DC but shorts the microphone to the amplifier at higher frequencies.

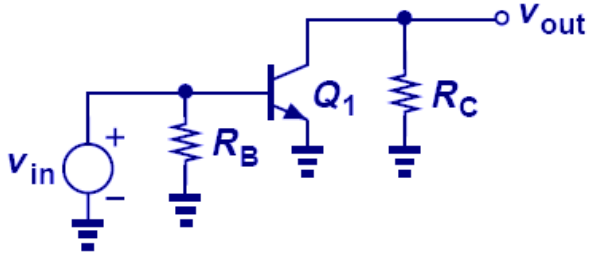
DC and AC Analysis



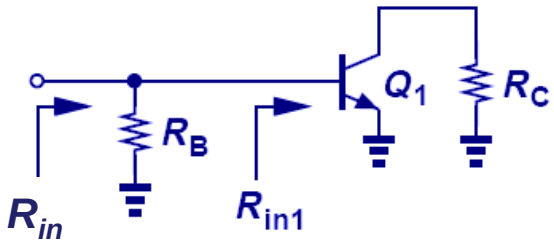
(a)



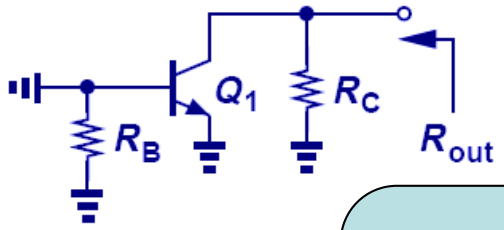
(b)



(c)



(d)



(e)

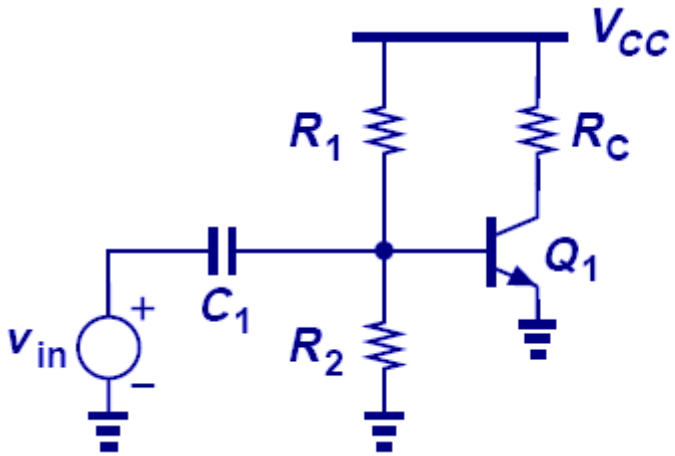
$$A_v = -g_m(R_C \parallel r_O)$$

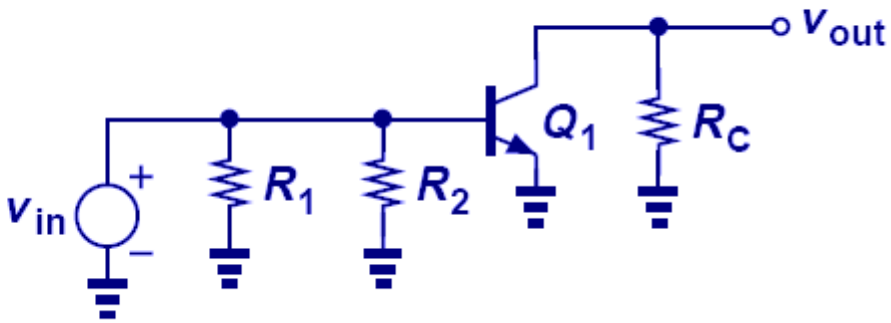
$$R_{in} = r_\pi \parallel R_B$$

$$R_{out} = R_C \parallel r_O$$

- Coupling capacitor is open for DC calculations and shorted for AC calculations.

CE Stage with Biasing



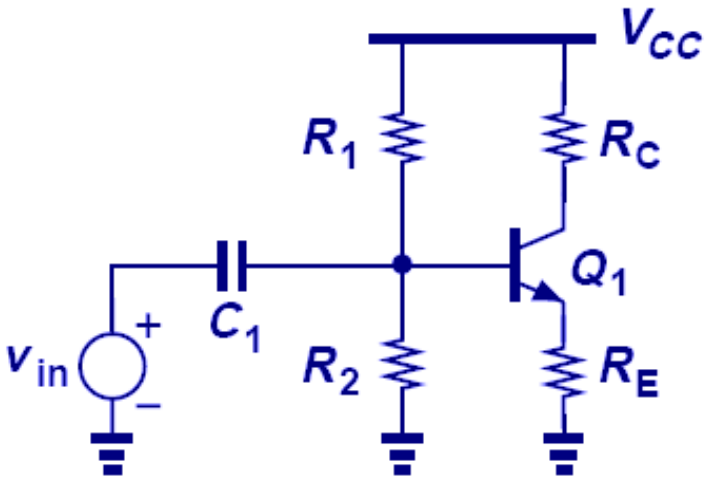


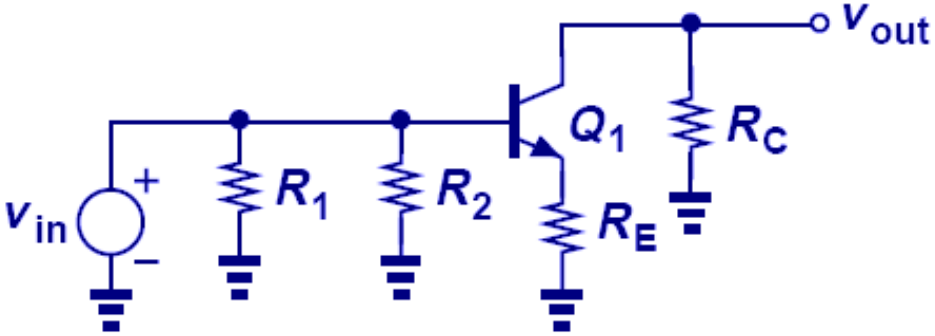
$$A_v = -g_m(R_C \| r_O)$$

$$R_{in} = r_\pi \| R_1 \| R_2$$

$$R_{out} = R_C \| r_O$$

CE Stage with Robust Biasing



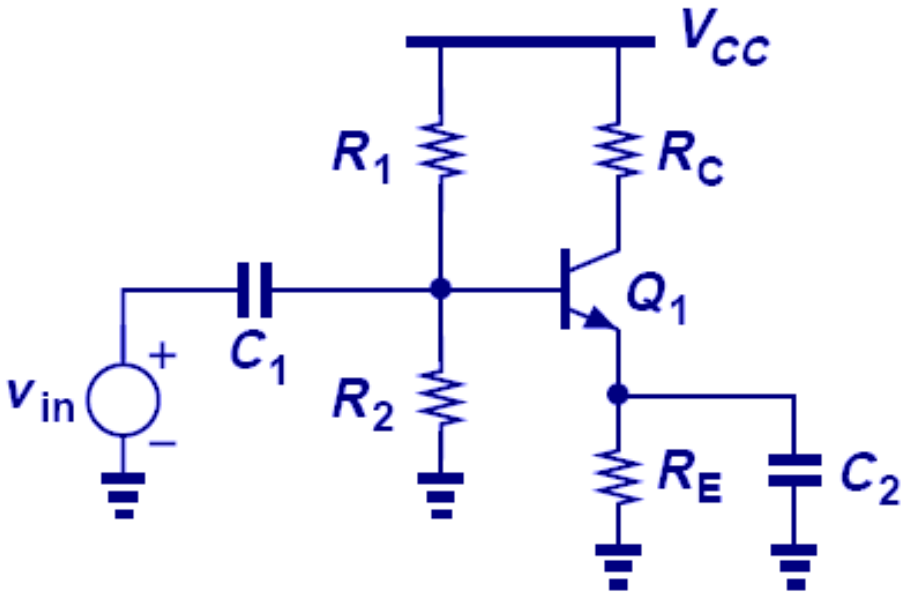


$$A_v = \frac{-R_C}{\frac{1}{g_m} + R_E}$$

$$R_{in} = [r_\pi + (\beta + 1)R_E] \| R_1 \| R_2$$

$$R_{out} = R_C$$

Removal of Degeneration for Signals at AC



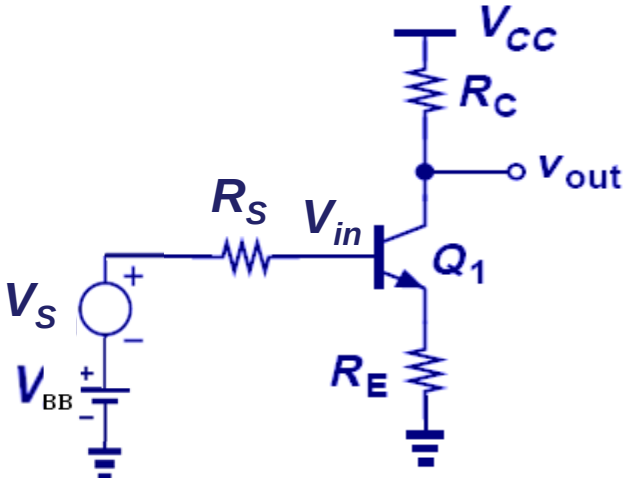
$$A_v = -g_m R_C$$

$$R_{in} = r_\pi \,||\, R_1 \,||\, R_2$$

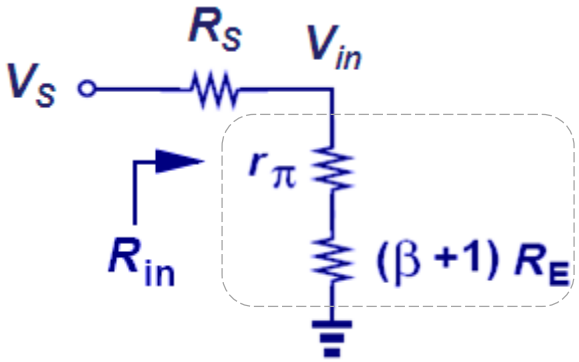
$$R_{out} = R_C$$

- Capacitor shorts out R_E at higher frequencies and removes degeneration.

Source Resistance



ac:



$$\frac{v_{out}}{v_s} = \frac{v_{in}}{v_s} \cdot \frac{v_{out}}{v_{in}}$$

$$\frac{v_{in}}{v_s} = \frac{R_{in}}{R_{in} + R_S}$$

$$R_{in} = r_\pi + (\beta+1)R_E$$

$$R_{out} = R_C$$

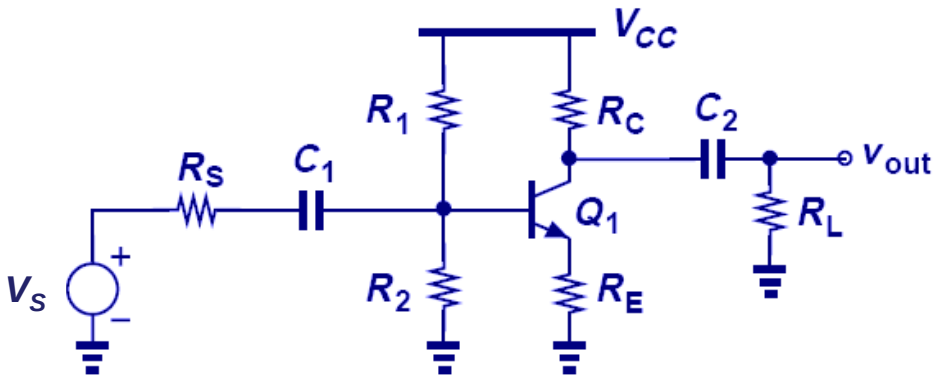
$$V_A = \infty$$

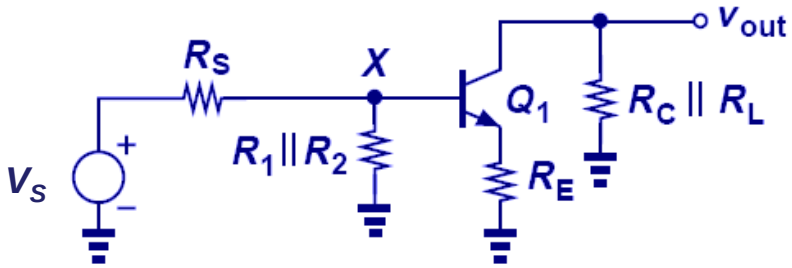
$$\frac{v_{out}}{v_s} = \frac{v_{in}}{v_s} \cdot \frac{v_{out}}{v_{in}}$$

$$\frac{v_{out}}{v_s} = \frac{-\beta R_C}{r_\pi + (\beta+1)R_E + R_S}$$

$$A_v = \frac{v_{out}}{v_s} \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_S}{\beta+1}}$$

Complete CE Stage





$$R_{in} = \left[r_\pi + (\beta + 1)R_E\right] \parallel R_1 \parallel R_2$$

$$R_{out} = R_C$$

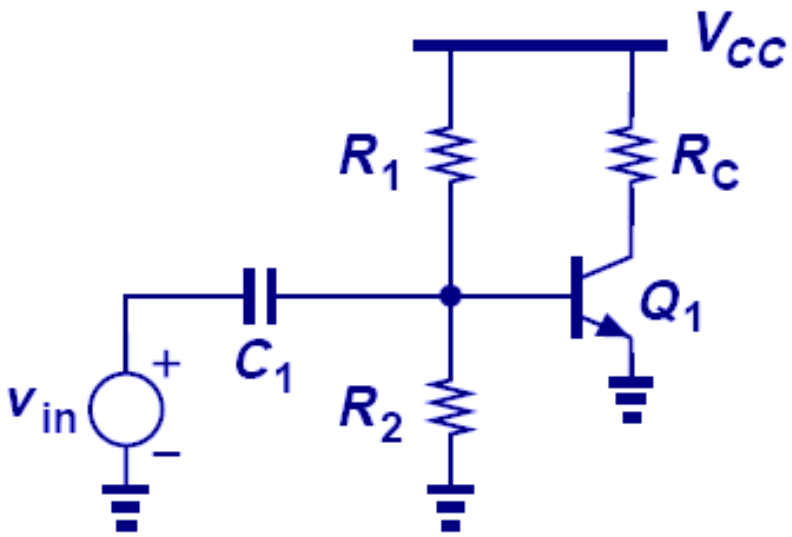
$$A_v = \frac{R_{in}}{R_{in} + R_S} \times \frac{-R_C \parallel R_L}{\frac{1}{g_m} + R_E}$$

The input signal source exhibits a finite resistance R_S and the output is tied to a load R_L.

Example

- A transistor is biased at a collector current of 1 mA. Determine the small-signal parameters if
- $\beta=100$
- $V_A=10$ V

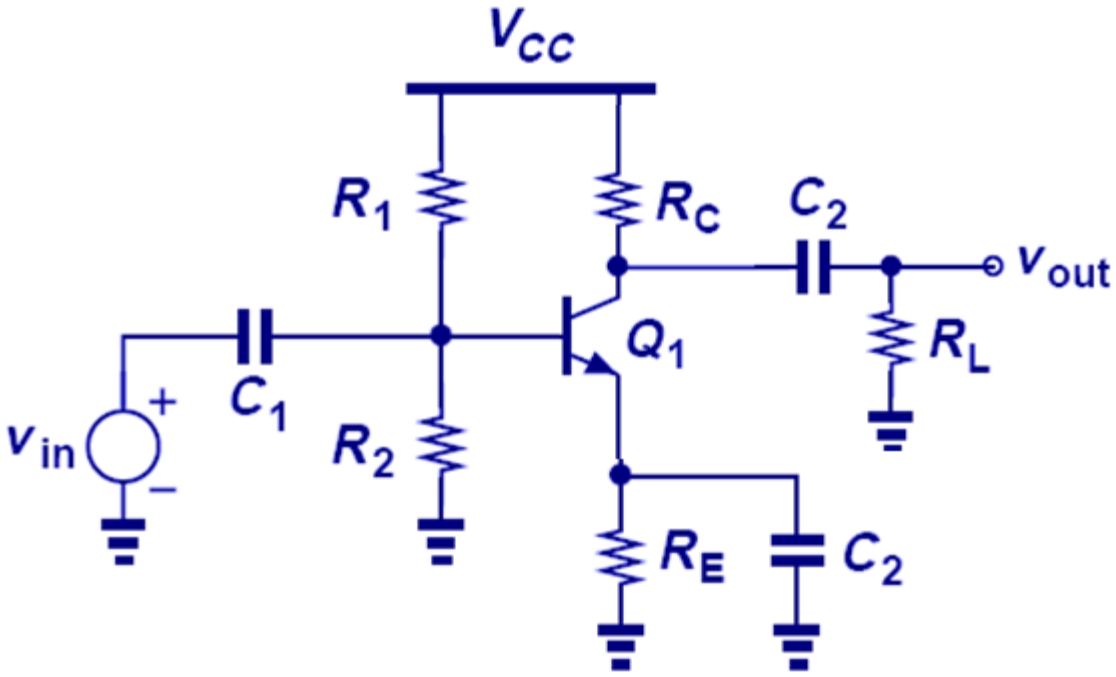
Example



- $\beta=100$
- $V_{CC}=1.4V$
- $I_{CQ}=1\ mA$
- $R_C=0.5K\ \Omega$
- $R_1=R_2=100K\ \Omega$
- $V_A=10\ V$

- R_{in}, R_{out}, A_V:?

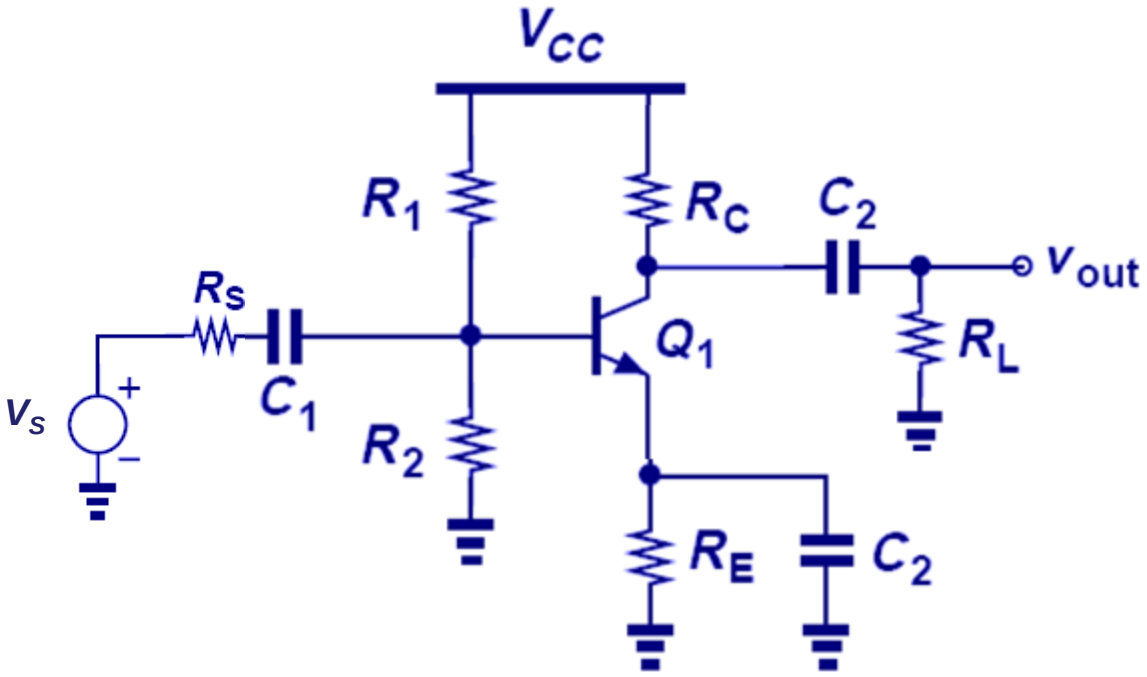
Example



- $\beta = 100$
- $V_{BE\ ON} = 0.7$ V
- $V_{CC} = 5.4$ V
- $R_1 = R_2 = 200$ K Ω
- $R_E = 1$ K Ω
- $R_C = 0.5$K Ω
- $R_L = 10$K Ω
- $V_A = 15$V

- R_{in}, R_{out}, A_V:?
- If $R_S = 100$ Ω , R_{in}, R_{out}, A_V:?

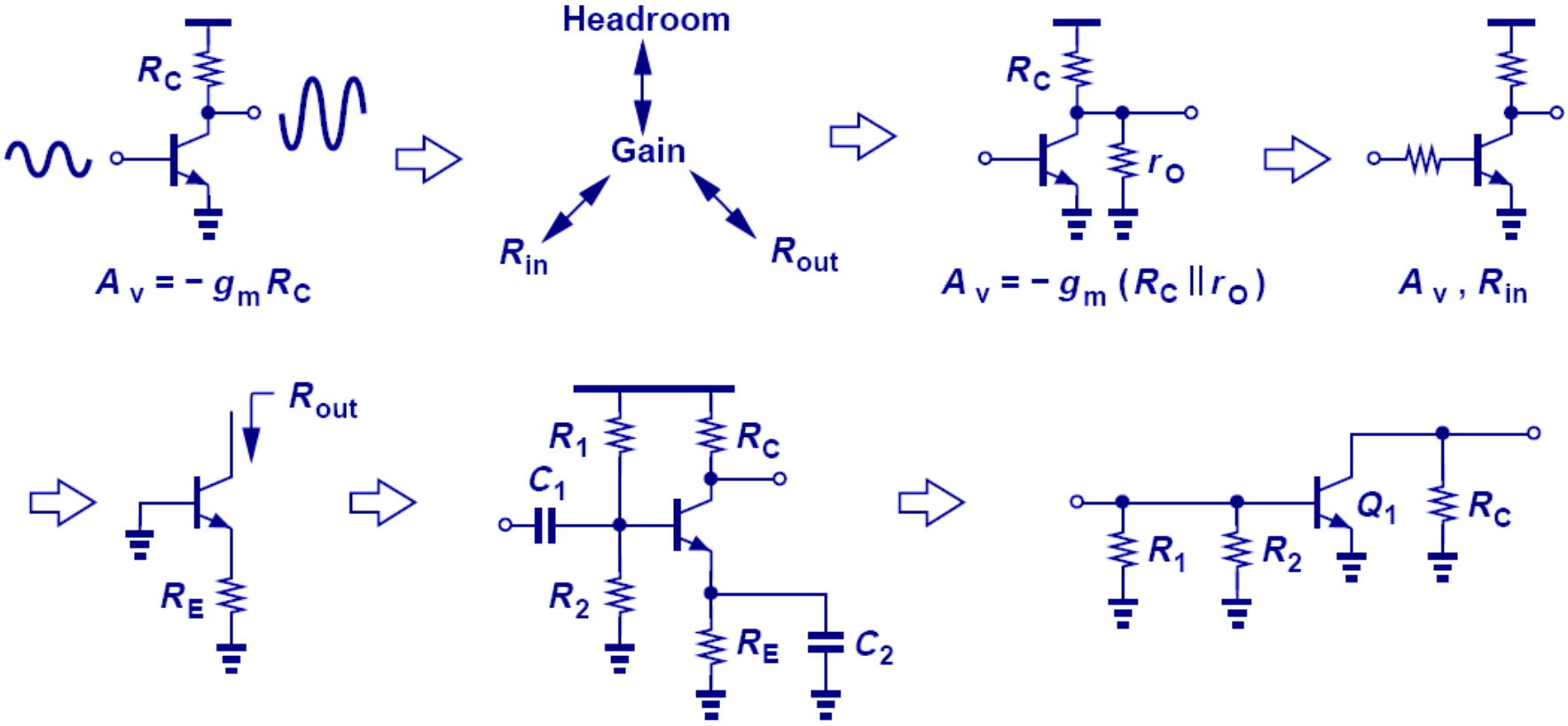
Example



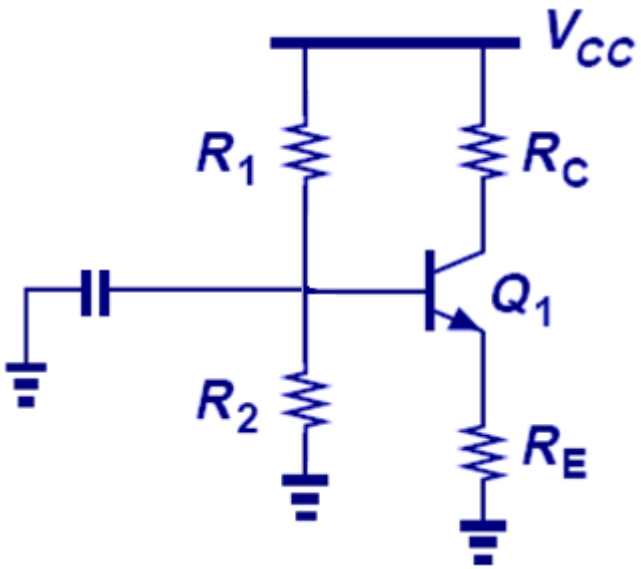
- $\beta = 100$
- $V_{BE\ ON} = 0.7$ V
- $V_{CC} = 5.4$ V
- $R_1 = R_2 = 200$ K Ω
- $R_E = 1$ K Ω
- $R_C = 0.5$K Ω
- $R_L = 10$K Ω
- $V_A = 15$V

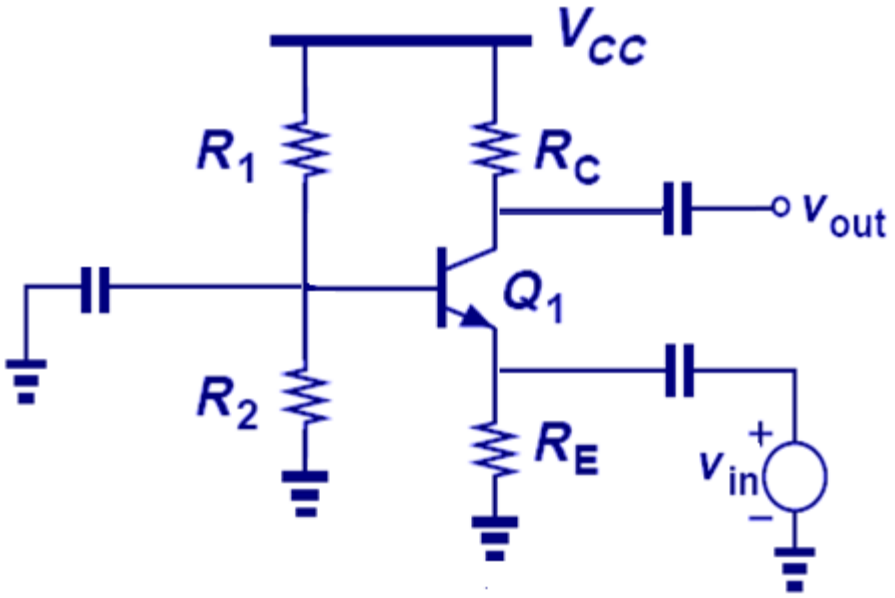
- R_{in}, R_{out}, A_V:?
- If $R_S = 100$ Ω , R_{in}, R_{out}, A_V:?
- Max Vs : Q1:active

Summary of CE Concepts



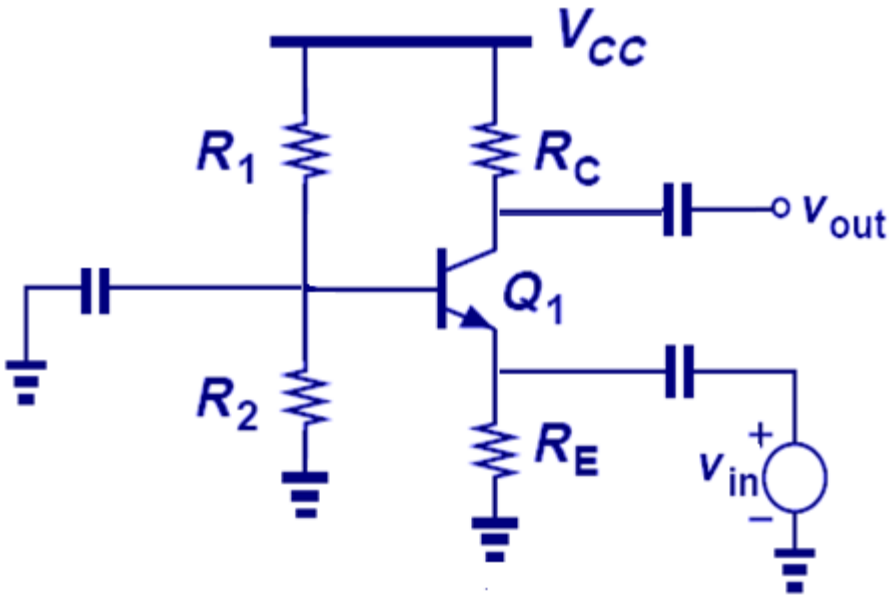
Common Base (CB) Amplifier

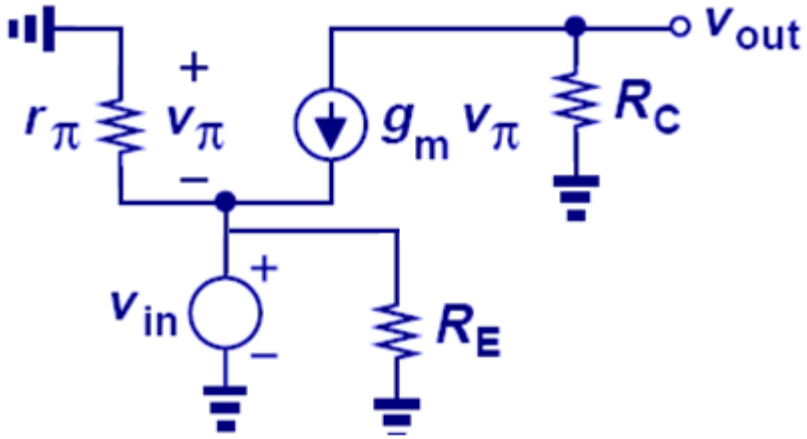




- In common base topology, where the base terminal is biased with a fixed voltage, emitter is fed with a signal, and collector is the output.

A_V for CB Stage

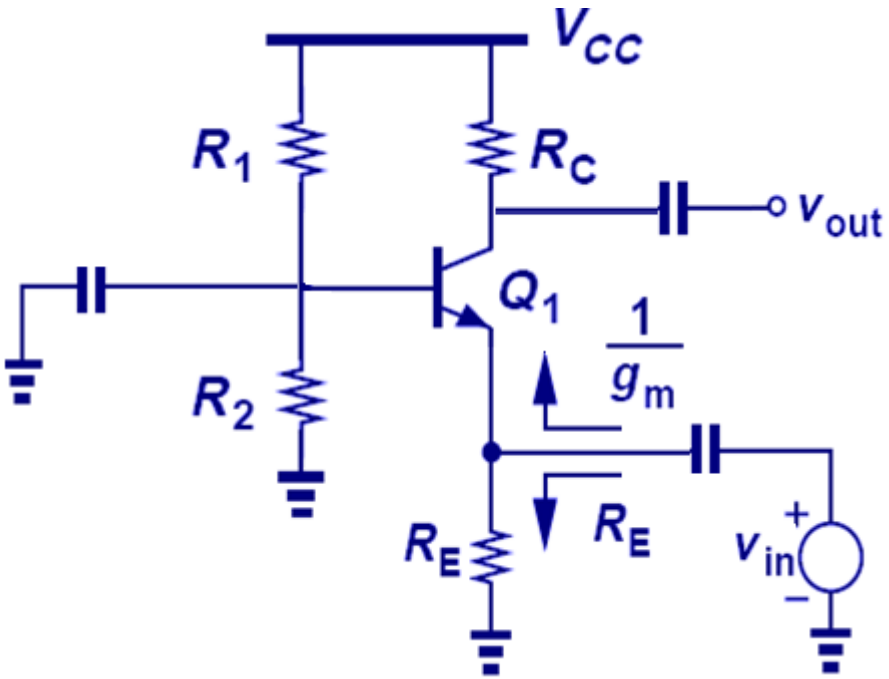




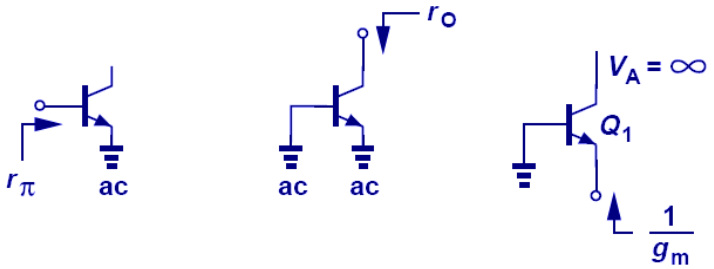
$$A_v = g_m R_C$$

- The voltage gain of CB stage is $g_m R_C$, which is identical to that of CE stage in magnitude and opposite in phase.

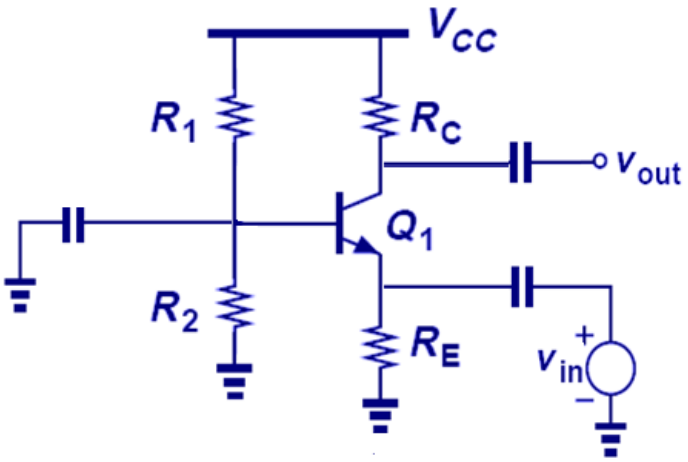
Input Impedance for CB Stage

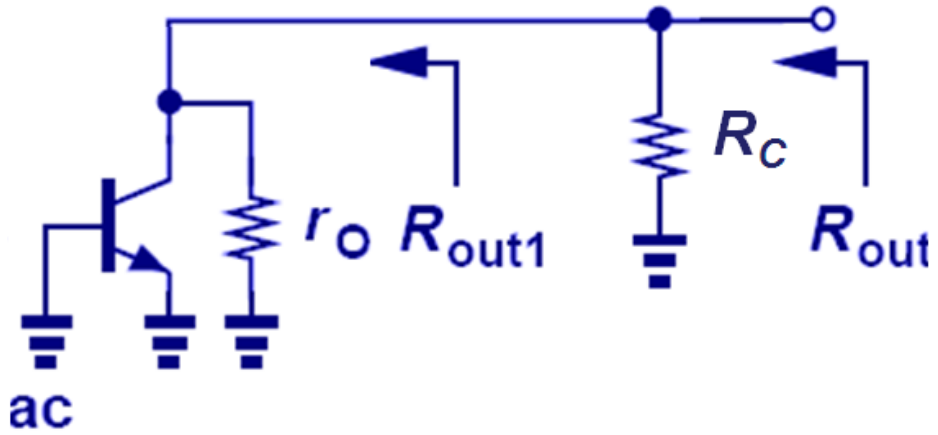


$$R_{in} = \frac{1}{g_m} \parallel R_E$$



Output Impedance of CB Stage

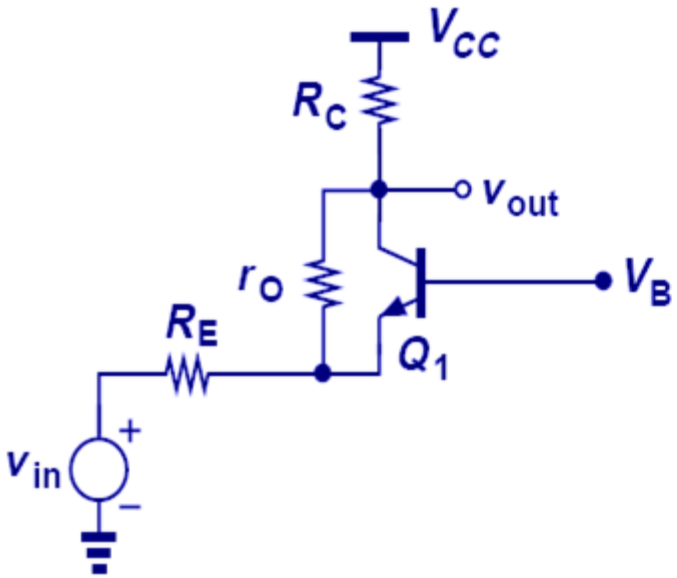


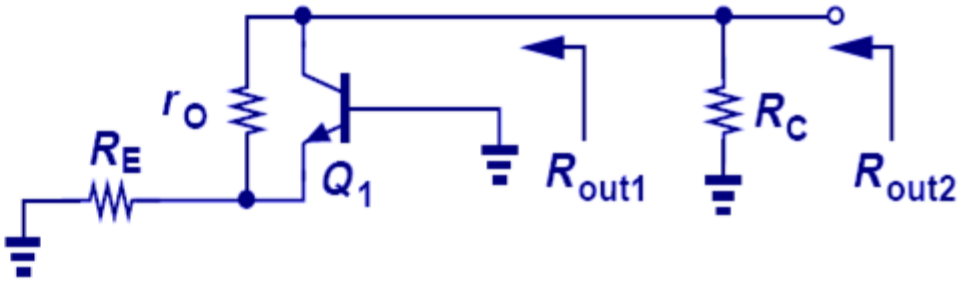


$$R_{out} = r_O \,||\, R_C$$

- The output impedance of CB stage is similar to that of CE stage.

Realistic Output Impedance of CB Stage





With Early effect

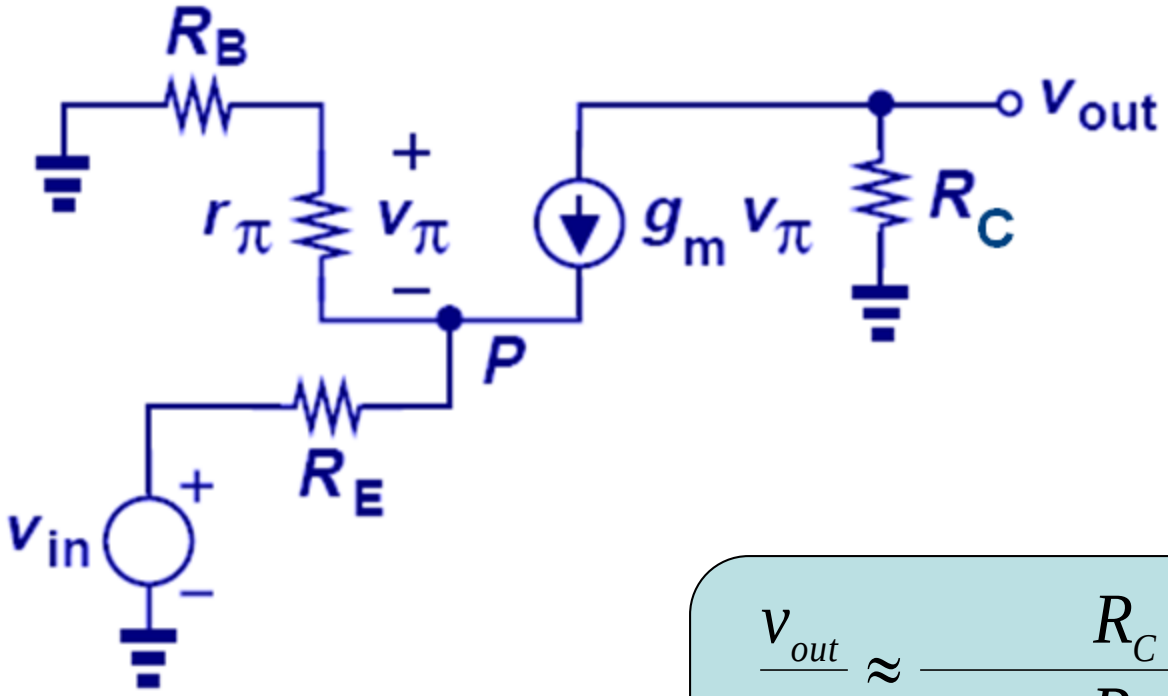
(VA<∞)

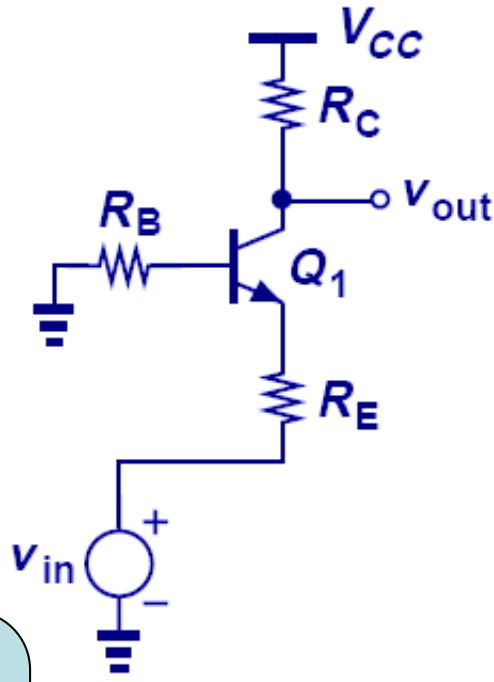
$$R_{out1} = \left[1 + g_m (R_E \,||\, r_\pi)\right] r_O + (R_E \,||\, r_\pi)$$

$$R_{out} = R_C \,||\, R_{out1}$$

- The output impedance of CB stage is equal to R_C in parallel with the impedance looking down into the collector.

A_v of CB with Base Resistance



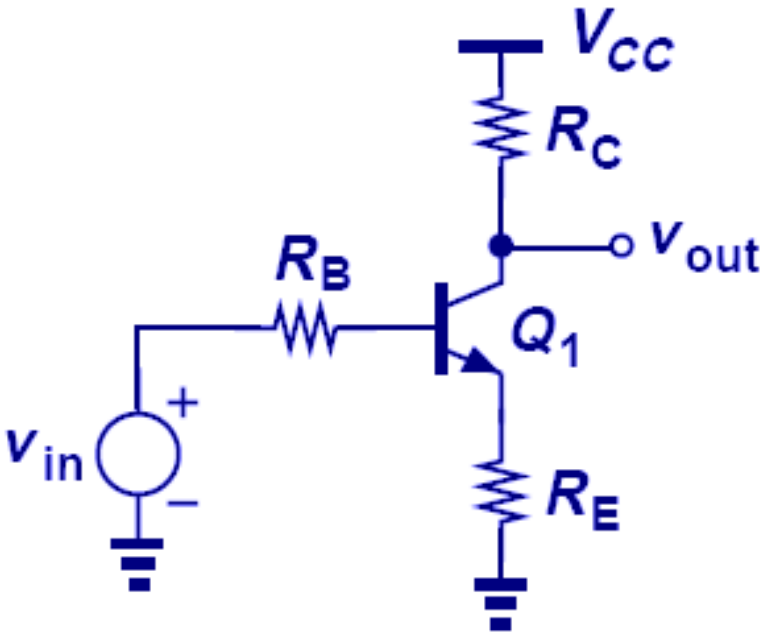


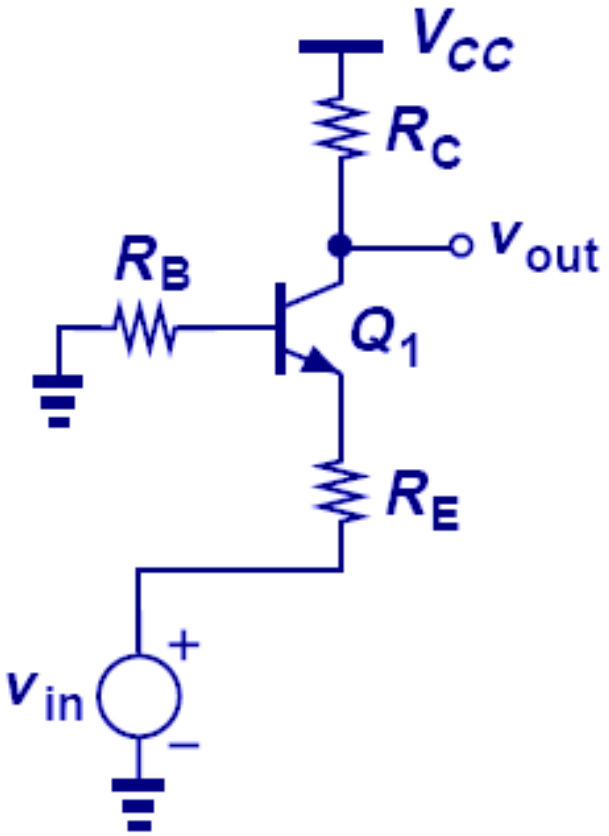
$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

- With an addition of base resistance, the voltage gain degrades.

Without Early effect ($V_A \to \infty$)

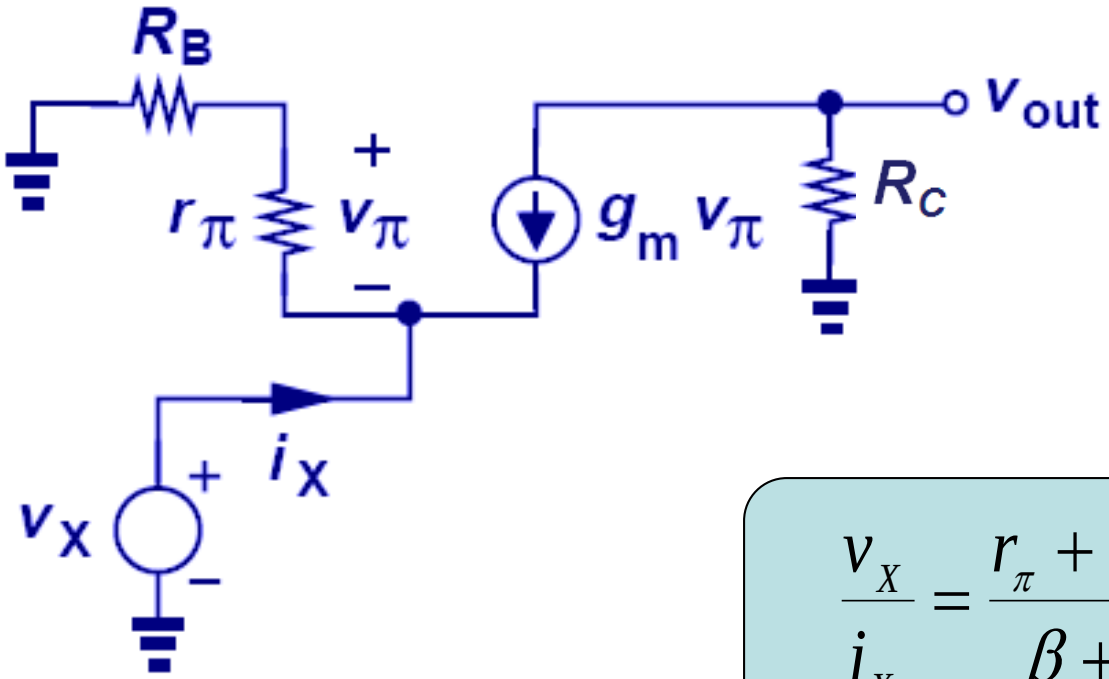
Comparison of CE and CB Stages with Base Resistance

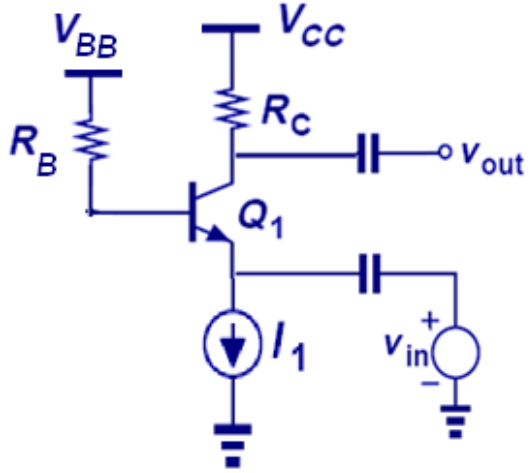




- The voltage gain of CB amplifier with base resistance is exactly the same as that of CE stage with base resistance and emitter degeneration, except for a negative sign.

Input Impedance of CB Stage with Base Resistance



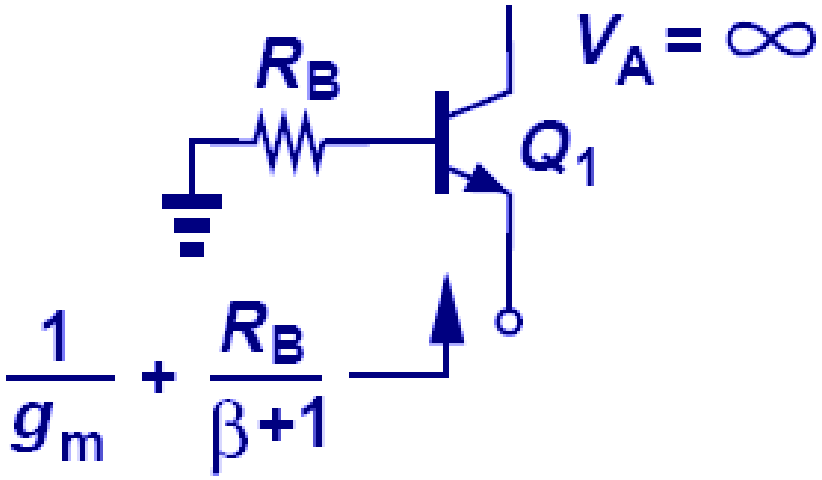


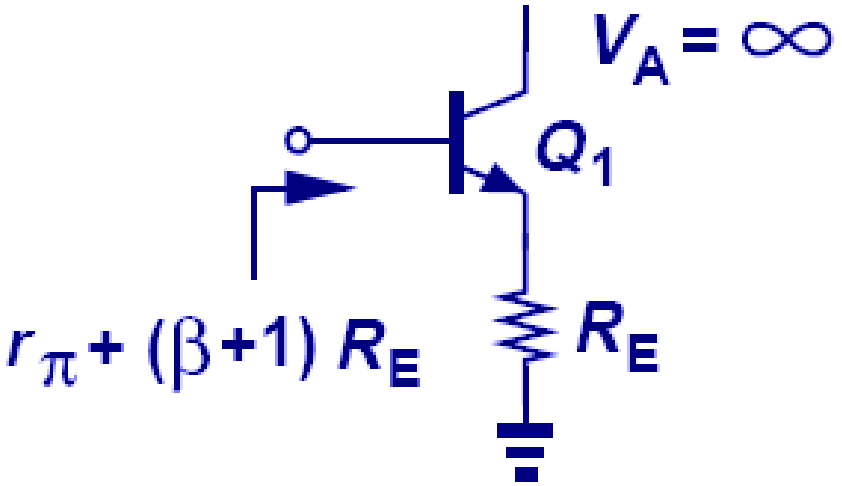
$$\frac{v_X}{i_X} = \frac{r_\pi + R_B}{\beta + 1} \approx \frac{1}{g_m} + \frac{R_B}{\beta + 1}$$

- The input impedance of CB with base resistance is equal to $1/g_m$ plus R_B divided by (β+1). This is in contrast to degenerated CE stage, in which the resistance in series with the emitter is *multiplied* by (β+1) when seen from the base.

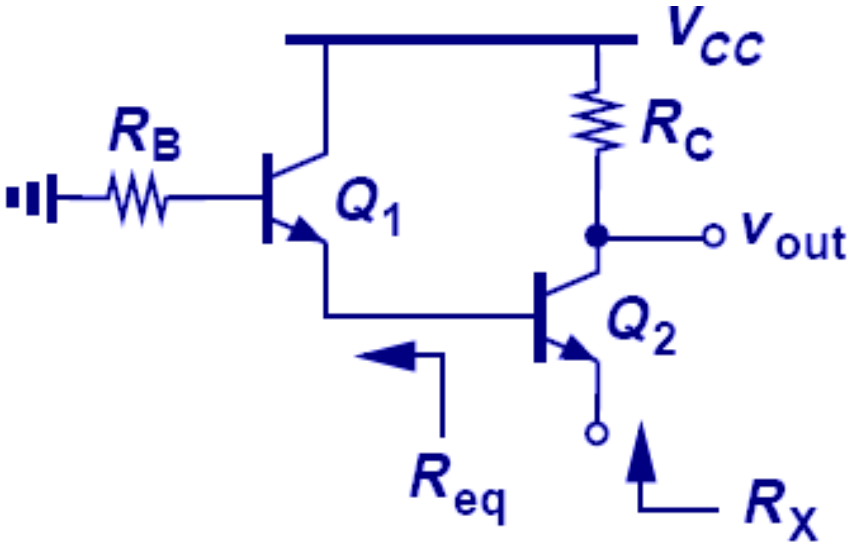
Without Early effect (VA→∞)

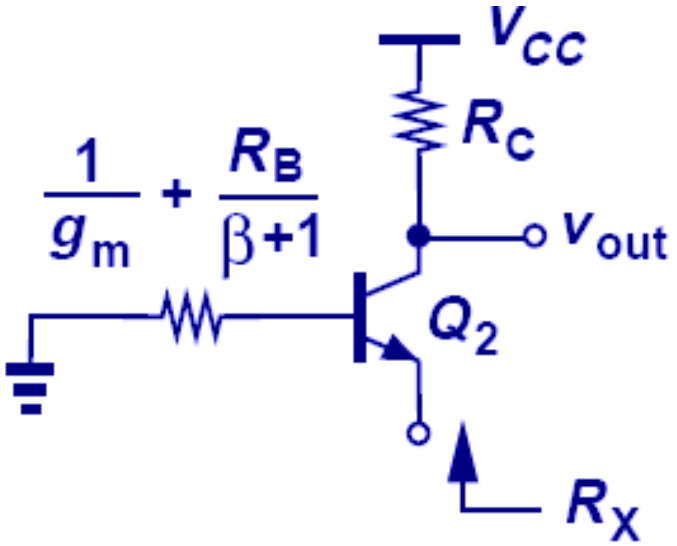
Input Impedance Seen at Emitter and Base





Input Impedance Example

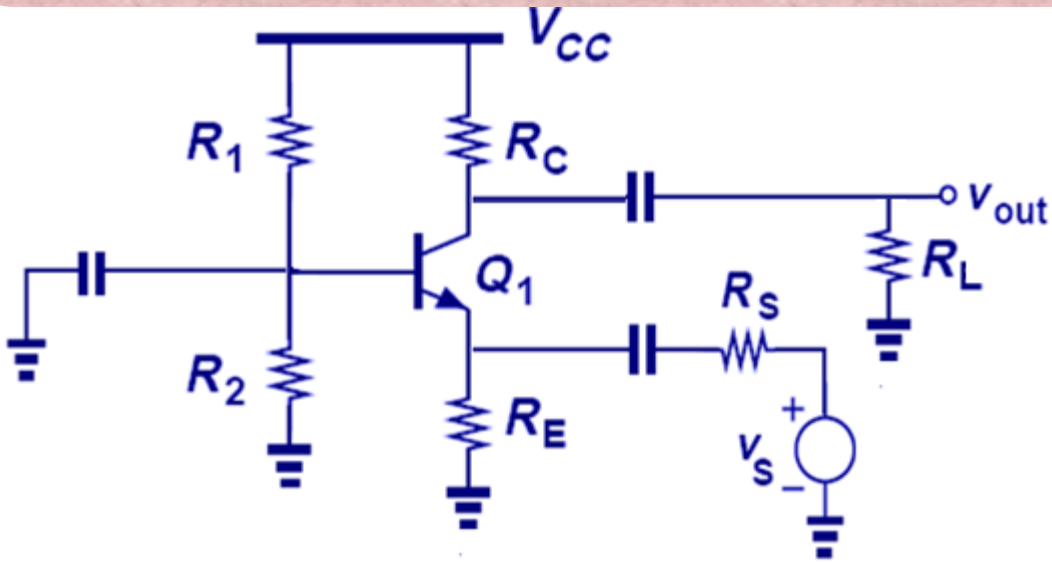




$$R_X = \frac{1}{g_{m2}} + \frac{1}{\beta+1}\left(\frac{1}{g_{m1}} + \frac{R_B}{\beta+1}\right)$$

- To find the R_X, we have to first find $R_{eq,}$ treat it as the base resistance of Q_2 and divide it by (β+1).

Example



- $\beta = 100$
- $V_{BE\ ON} = 0.7\ V$
- $V_{CE\ sat} = 0.2\ V$
- $V_{CC} = 12\ V$
- $R_1 = R_2 = 20\ K\Omega$
- $R_E = 1\ K\Omega$
- $R_C = 1\ K\Omega$
- $R_L = 1K\ \Omega$
- $R_S = 10\ \Omega$

$$I_C = 4.8\,mA \Rightarrow V_{CE\,Q} = 12 - 2 \times 4.8 = 1.7 > 0.2V \Rightarrow active$$

$$g_m = 192\,mS \Rightarrow \frac{1}{g_m} = 5.1\Omega$$

$$R_{in} = \frac{1}{g_m} \| R_E \approx 5.1\Omega$$

$$R_{out} \approx R_C = 1K\Omega$$

$$A_v = g_m R_{c\ total} = g_m (R_c \| R_L) \approx 96$$

$$A_{Vs} = \frac{R_{in}}{R_{in} + R_S} \times A_V \approx 32$$

$$A_I = \frac{R_{in} + R_S}{R_L} A_{Vs} = 0.48$$

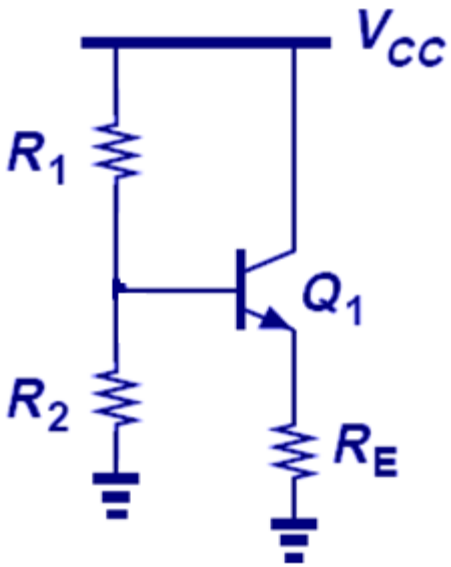
- $R_{in}, R_{out}, A_V, A_{Vs}, A_I$:?

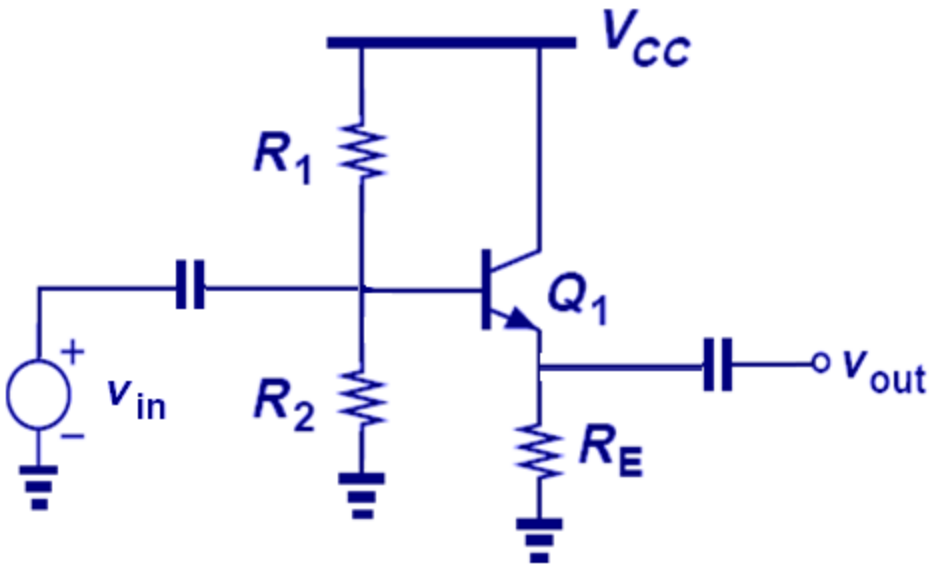
Course Overview

الکترونیک ۱

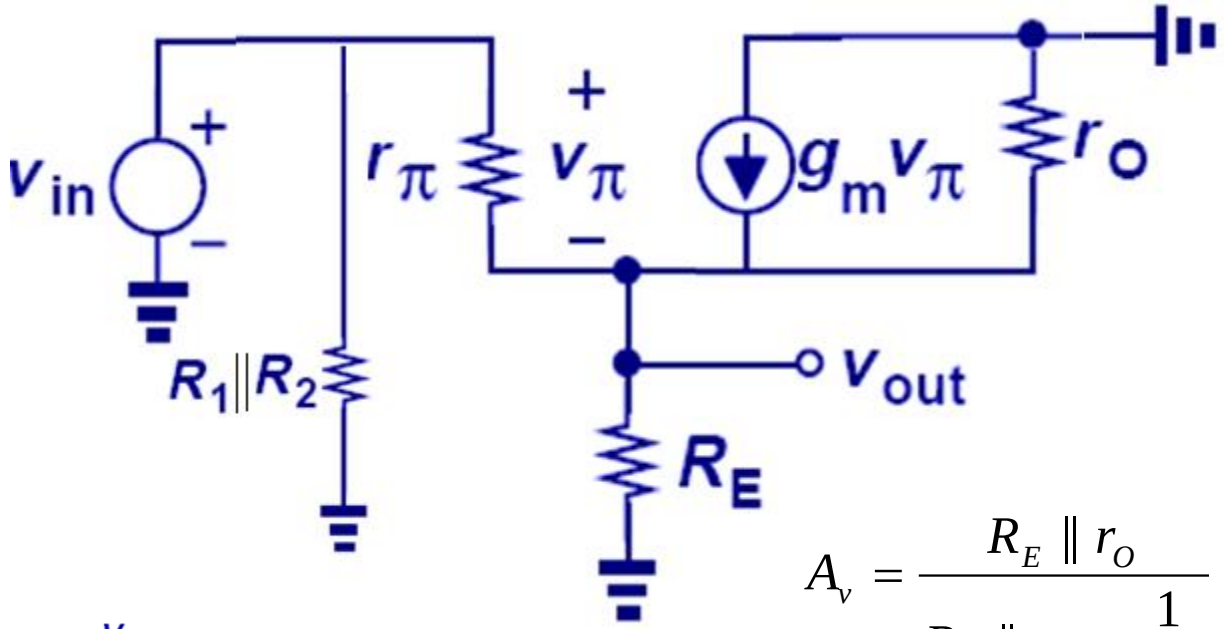
- Semiconductor physics
- PN junction
- BJT
  - BJT physics
  - dc analysis
  - ac/dc load lines
  - Stability
- **BJT : Small signal analysis**
  - **CE amplifier**
  - **CE amplifier**
  - **CC stage (emitter follower)**
- MOSFET

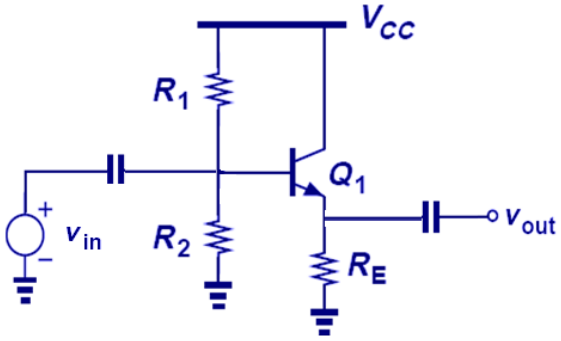
Emitter Follower (Common Collector Amplifier)





Small Signal Model of CE



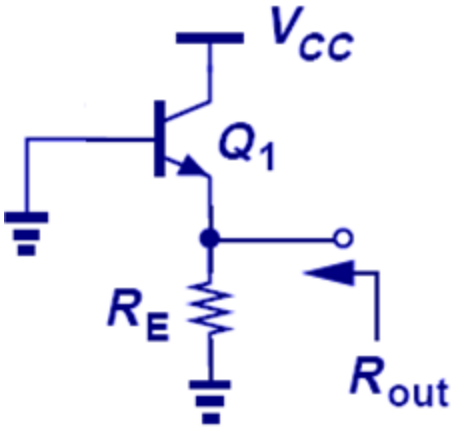


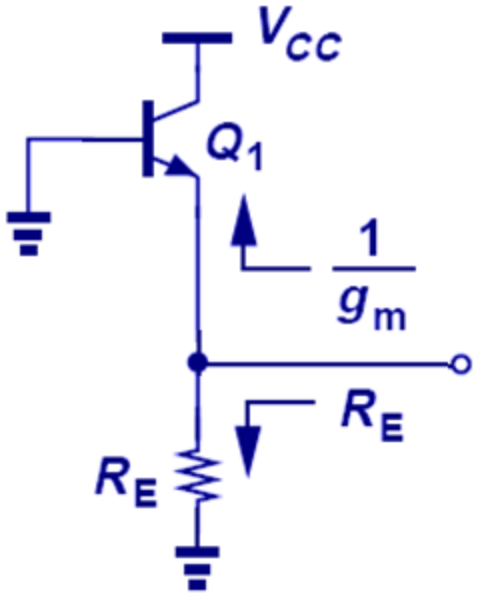
$$A_v = \frac{R_E \parallel r_O}{R_E \parallel r_O + \dfrac{1}{g_m}}$$

$$R_{in} = [r_\pi + (\beta + 1)(R_E \parallel r_O)] \parallel R_1 \parallel R_2$$

$$R_{out} = \frac{1}{g_m} \parallel R_E \parallel r_O$$

Output Impedance of Emitter Follower

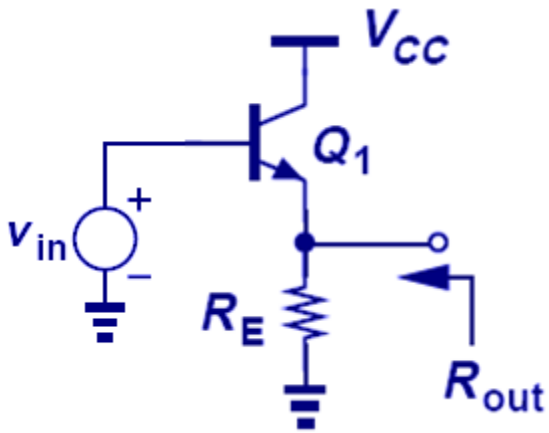


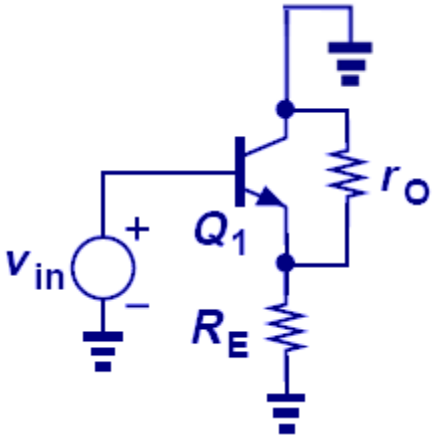


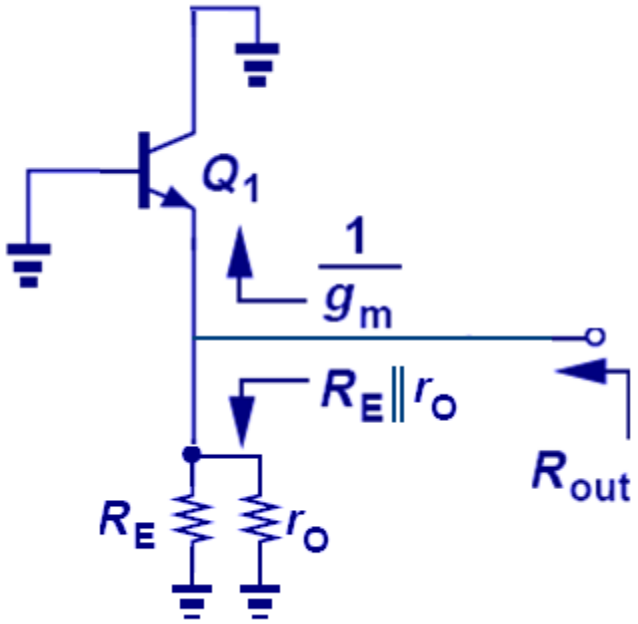
$$R_{out} = \frac{1}{g_m} \| R_E$$

(neglecting r_o)

Output Impedance of Emitter Follower (with Early effect)



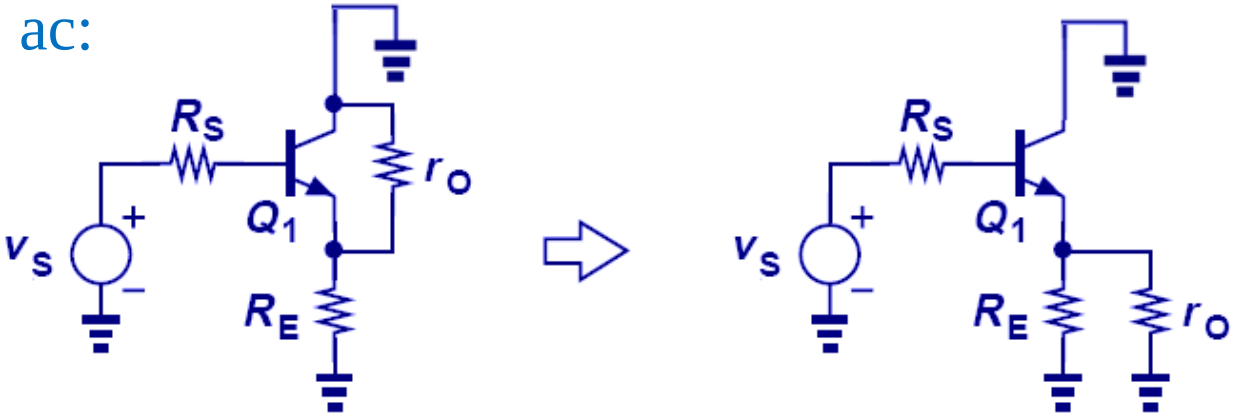




$$R_{out} = \frac{1}{g_m} \| R_E \| r_o$$

Emitter Follower with Source Resistance

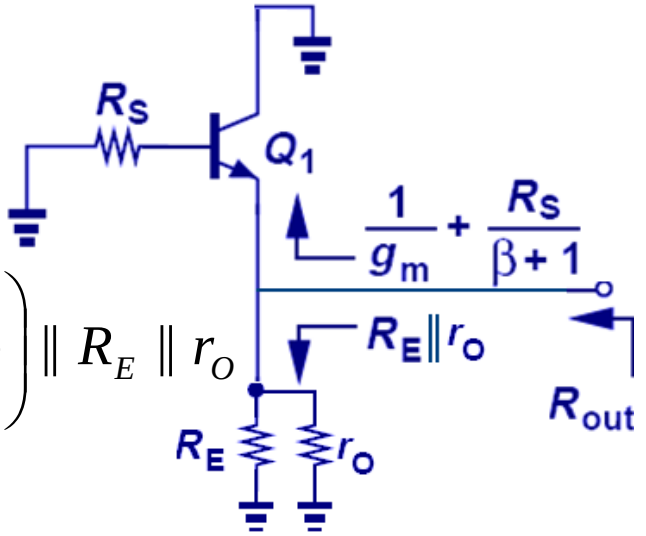
ac:



$$A_v = \frac{R_E \parallel r_O}{R_E \parallel r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}$$

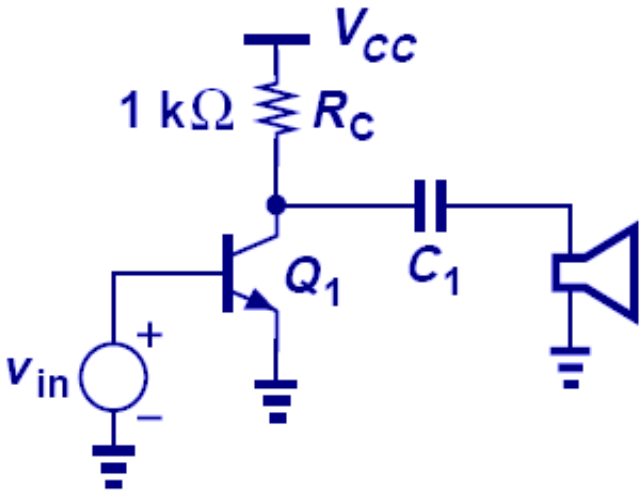
$$R_{in} = r_\pi + (\beta+1)(R_E \parallel r_O)$$

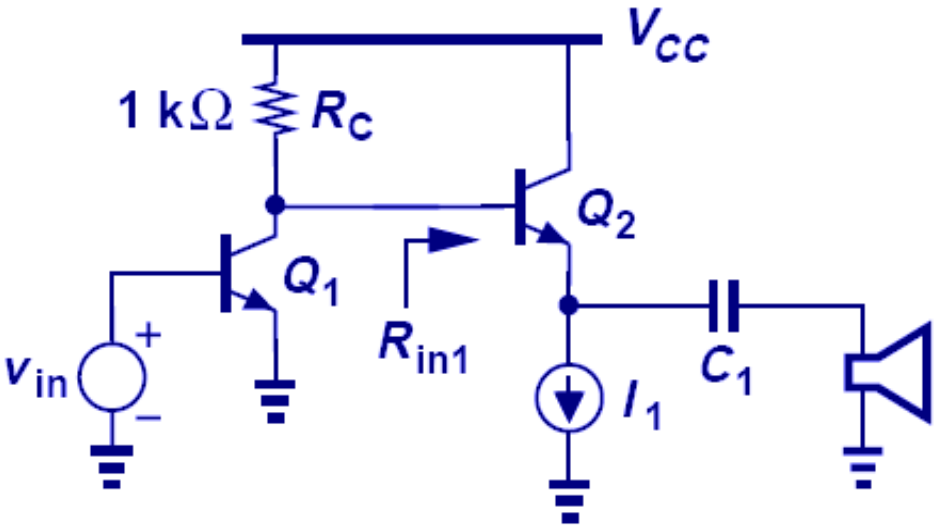
$$R_{out} = \left(\frac{R_s}{\beta+1} + \frac{1}{g_m}\right) \parallel R_E \parallel r_O$$



- Since r_O is in parallel with R_E, its effect can be easily incorporated into voltage gain and input and output impedance equations.

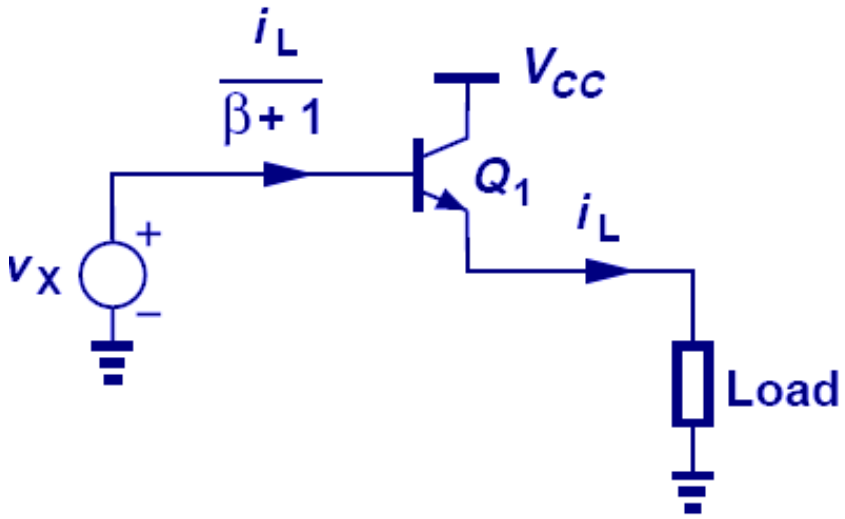
Emitter Follower as Buffer





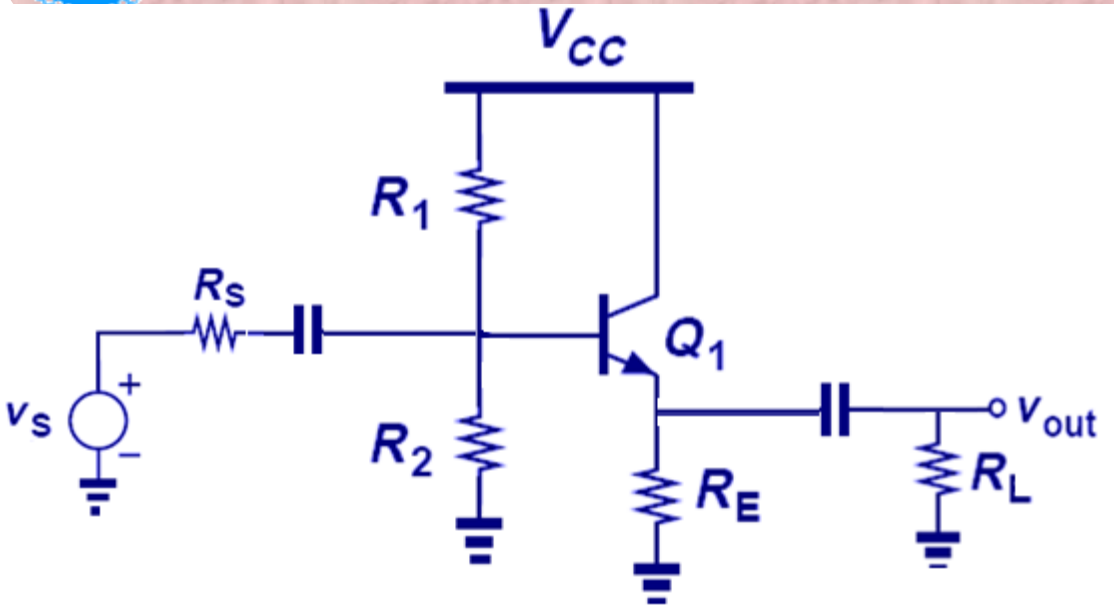
- Since the emitter follower increases the load resistance to a much higher value, it is suited as a buffer between a CE stage and a heavy load resistance to alleviate the problem of gain degradation.

Current Gain



- There is a current gain of (β+1) from base to emitter.
- Effectively speaking, the load resistance is multiplied by (β+1) as seen from the base.

Example



- $\beta = 50$
- $V_{BE\ ON} = 0.7$ V
- $V_{CE\ sat} = 0.2$ V
- $V_{CC} = 5$ V
- $R_1 \| R_2 = 500$ K Ω
- $R_E = 1$ KΩ
- $R_L = 2$ KΩ
- $R_S = 100$ Ω
- $r_\pi = 1.1$ KΩ

$$R_{in} = [r_\pi + (\beta + 1)(R_E \| R_L)] \| R_1 \| R_2 = 60.2\ K\Omega$$

$$R_{out} = \left(\frac{1}{g_m} + \frac{R_1 \| R_2 \| R_S}{\beta + 1}\right) \| R_E \approx 11.9\,\Omega$$

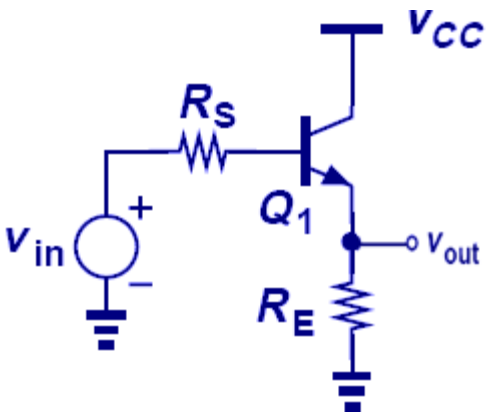
$$A_v = \frac{R_E \| R_L}{R_E \| R_L + \frac{1}{g_m}} \approx 0.98$$

$$A_{vs} = \frac{R_{in}}{R_{in} + R_S} A_v \approx 0.978$$

- R_{in}, R_{out}, A_V , A_I :?

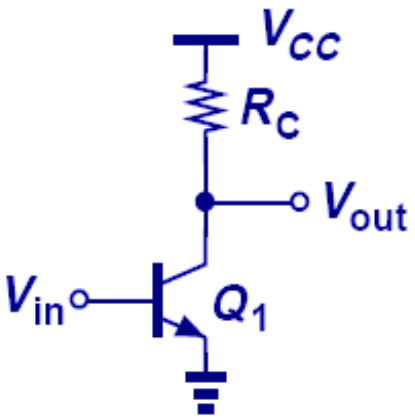
Small Signal of CC Amplifier

الکترونیک ۱

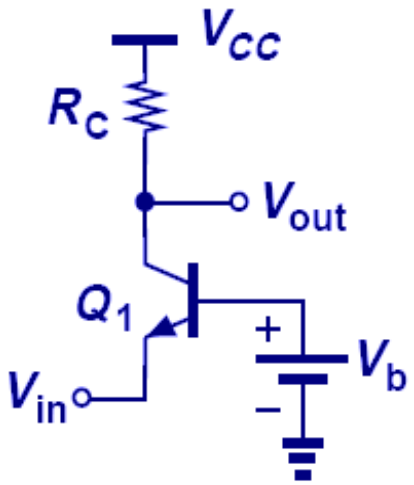
Without Early effect	With Early effect
	$A_v = \dfrac{R_E \parallel r_O}{R_E \parallel r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}$ $R_{in} = r_\pi + (\beta+1)(R_E \parallel r_O)$ $R_{out} = \left(\dfrac{R_s}{\beta+1} + \dfrac{1}{g_m}\right) \parallel R_E \parallel r_O$

Summary of Amplifier Topologies

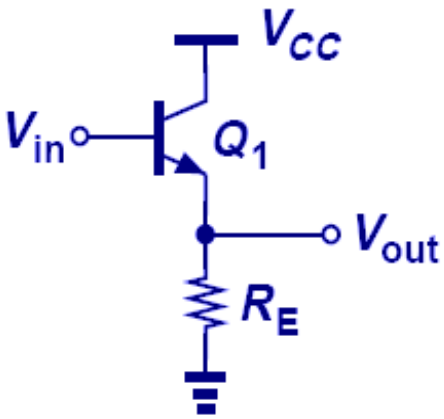
CE Stage



CB Stage

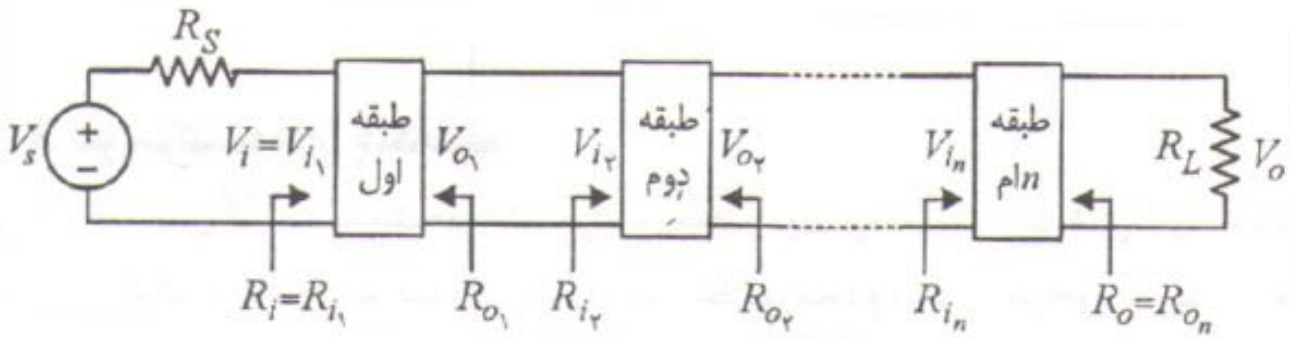


Follower



- The three amplifier topologies studied so far have different properties and are used on different occasions.
- CE and CB have voltage gain with magnitude greater than one, while follower's voltage gain is at most one.

Multi-Stage Amplifier



$$A_V=\frac{V_o}{V_i}=\frac{V_{o_n}}{V_{i_n}}\times\frac{V_{o_{n-1}}}{V_{i_{n-1}}}\times\ldots\times\frac{V_{o_2}}{V_{i_2}}\times\frac{V_{o_1}}{V_{i_1}}$$

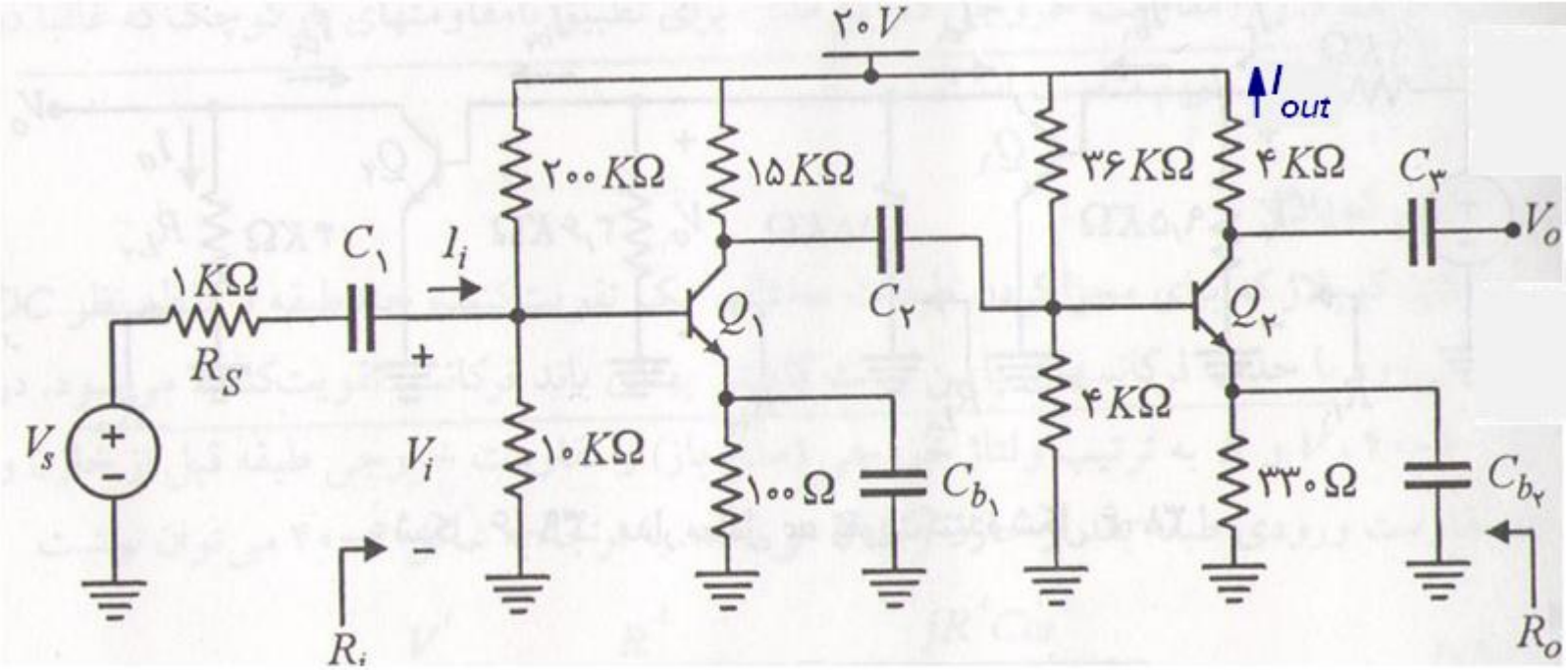
$$A_V=A_{V_n}\times A_{V_{n-1}}\times\ldots\times A_{V_2}\times A_{V_1}$$

$$A_I=A_{I_1}\times A_{I_2}\times\ldots\times A_{I_{n-1}}\times A_{I_n}$$

Calculating A_v and R_{in} for Stage 2:

Calculating R_{out} for Stage 2:

Multi-Stage Amplifier



- $\beta = 50$, $r_0 = 40\ k\Omega$

- R_{in}, R_{out}, A_V , A_I :?
- Max symmetric V_o swing?
- Max Vs swing?

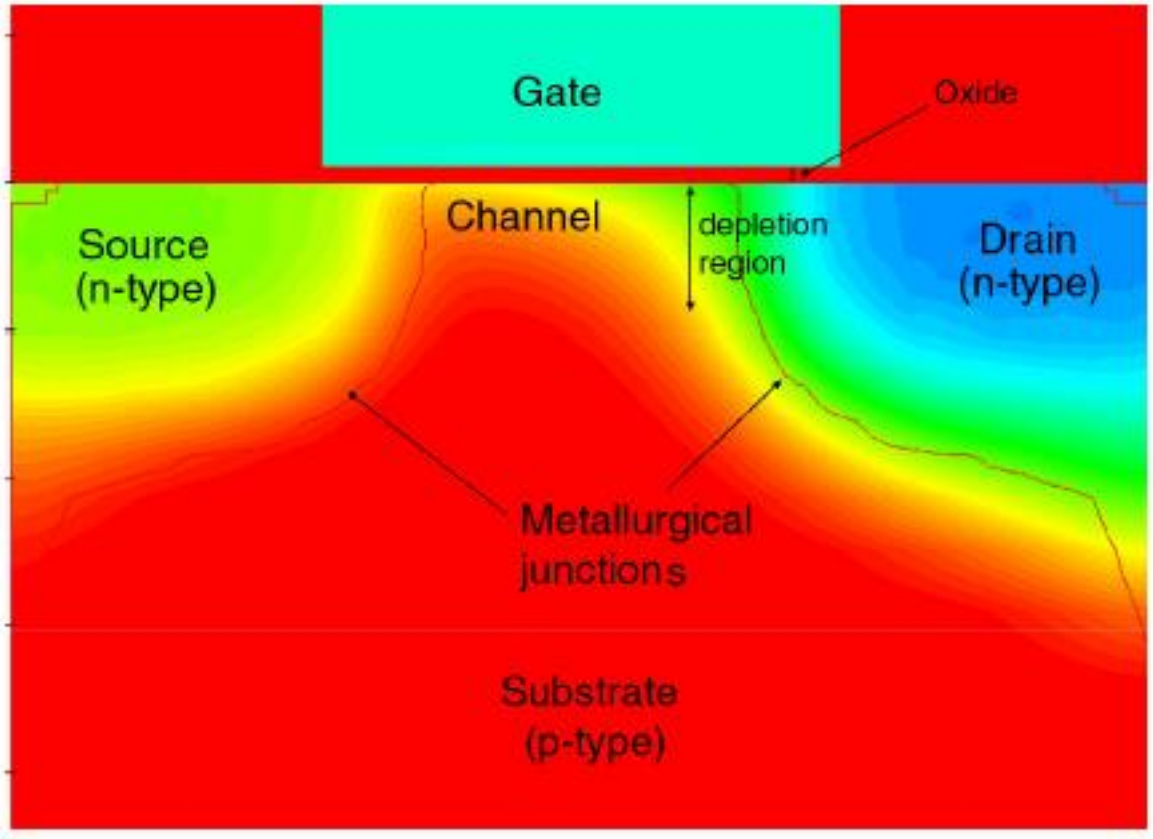
Course Overview

الکترونیک ۱

- Semiconductor physics
- PN junction
- BJT
- BJT : Small signal analysis
- **MOSFET** ← Chapter 6 : Physics of MOS Transistors

The MOSFET

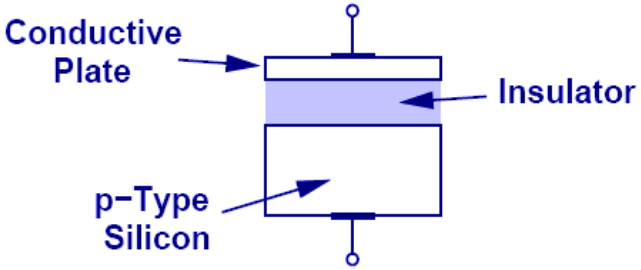
- No other human artifact has been fabricated in larger numbers ..
- "…some consider it one of the most important technological breakthroughs in human history…" (Wikipedia)

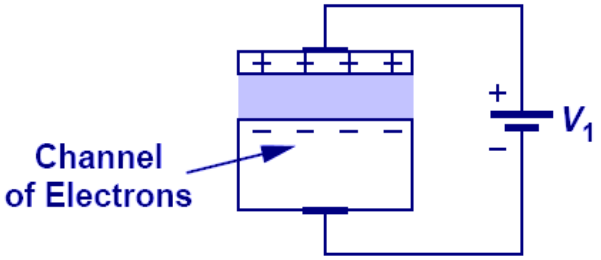


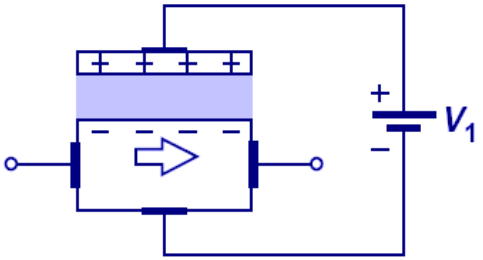
M. Fischetti, 2009

- Conceived ~ 1930
- First successful fabrication: late 1950s
- Mid 1980s: Power problem → low power device →CMOS
- Today *CMOS technology* is the dominant technology in electronics industry.

Metal-Oxide-Semiconductor (MOS) Capacitor

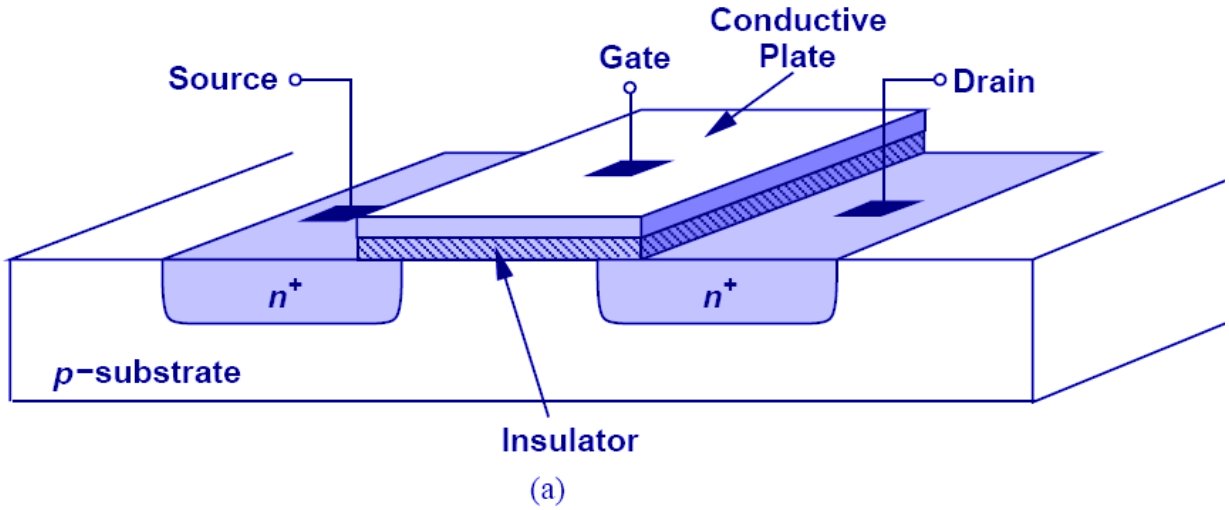




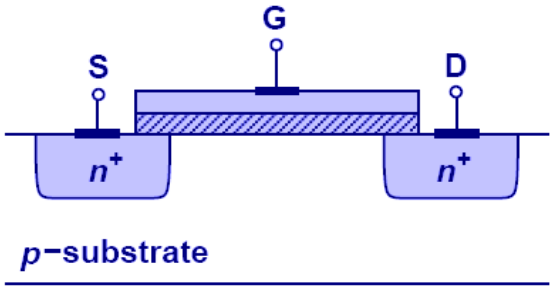


- The MOS structure can be thought of as a parallel-plate capacitor, with the top plate being the positive plate, oxide being the dielectric, and Si substrate being the negative plate. (We are assuming P-substrate.)

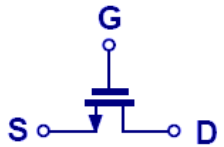
Structure and Symbol of MOSFET



(a)

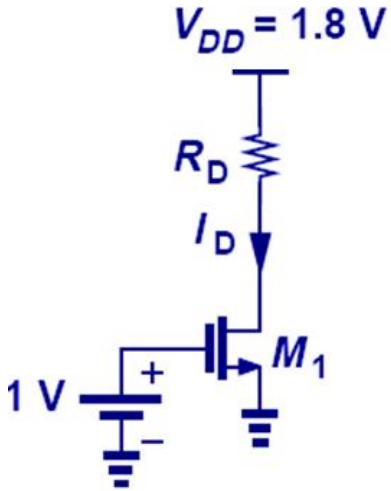


(b)



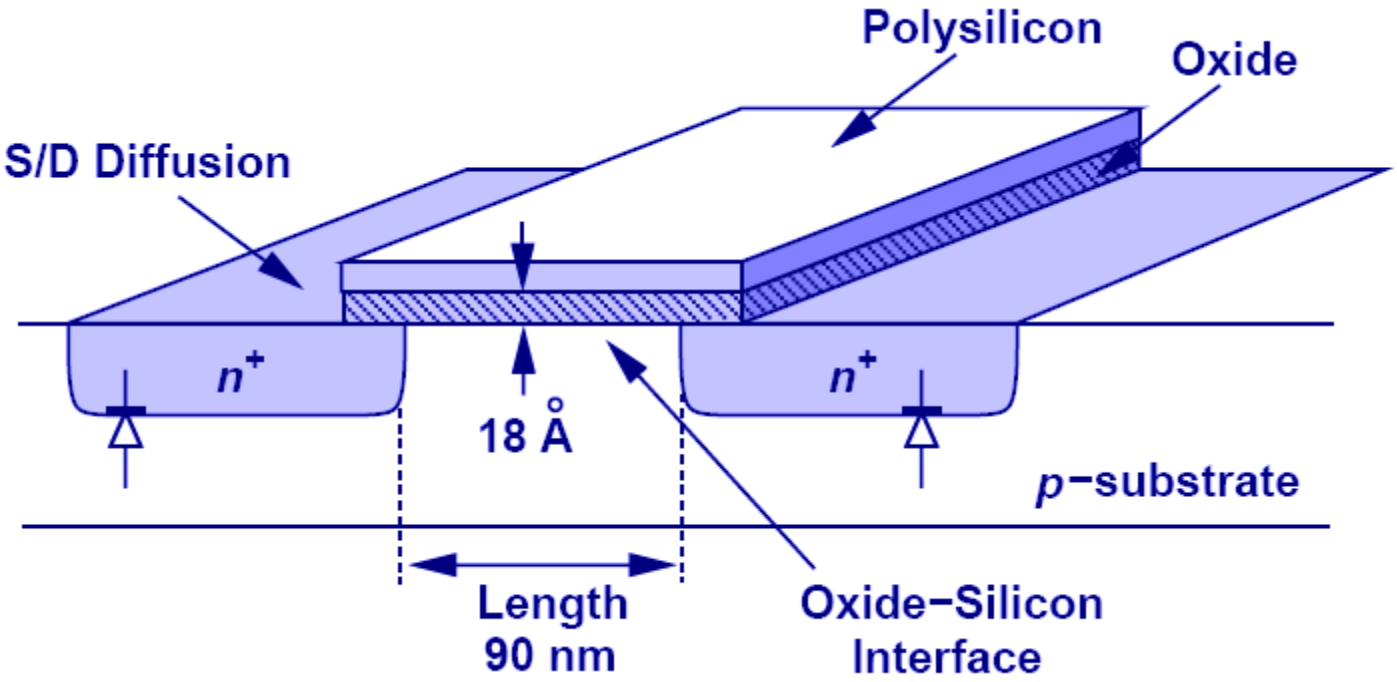
(c)

:NMOS



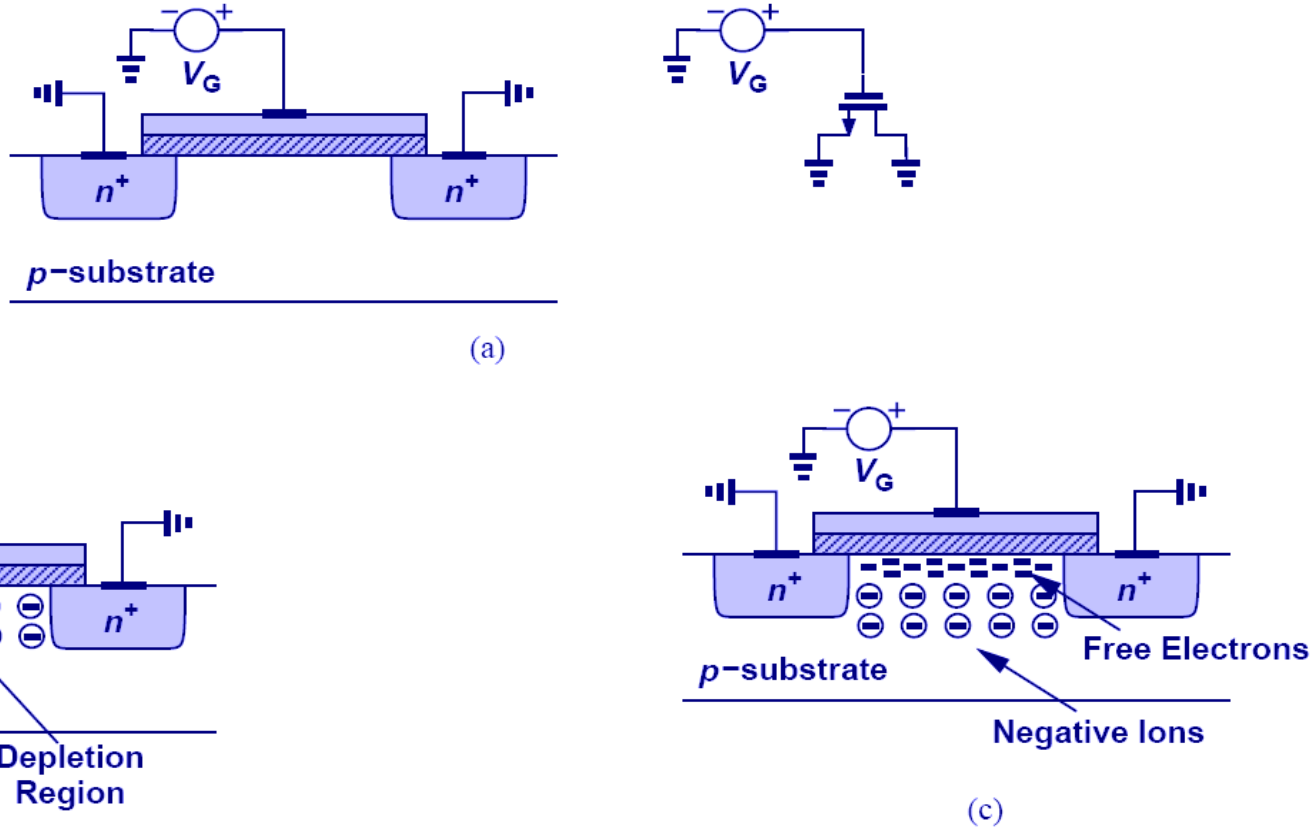
- This device is symmetric, so either of the n+ regions can be source or drain.

State of the Art MOSFET Structure



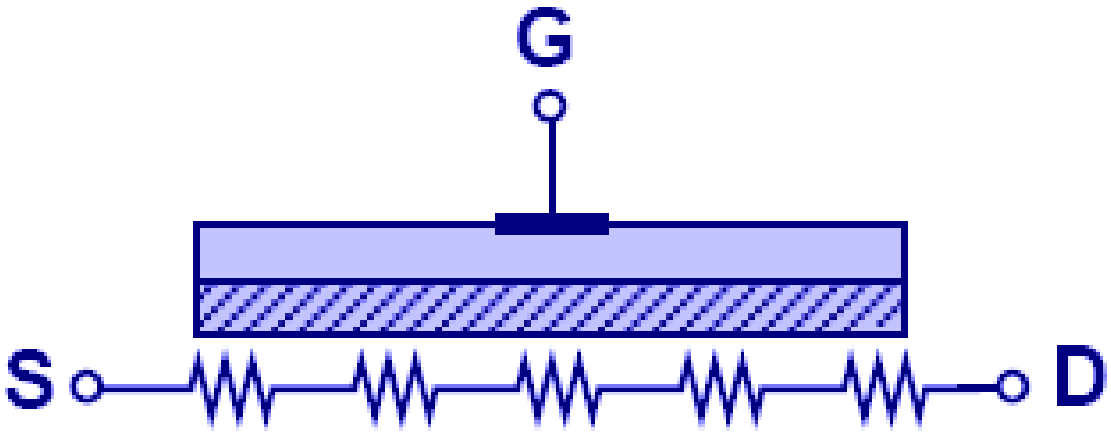
- The gate is formed by polysilicon, and the insulator by Silicon dioxide.

Formation of Channel



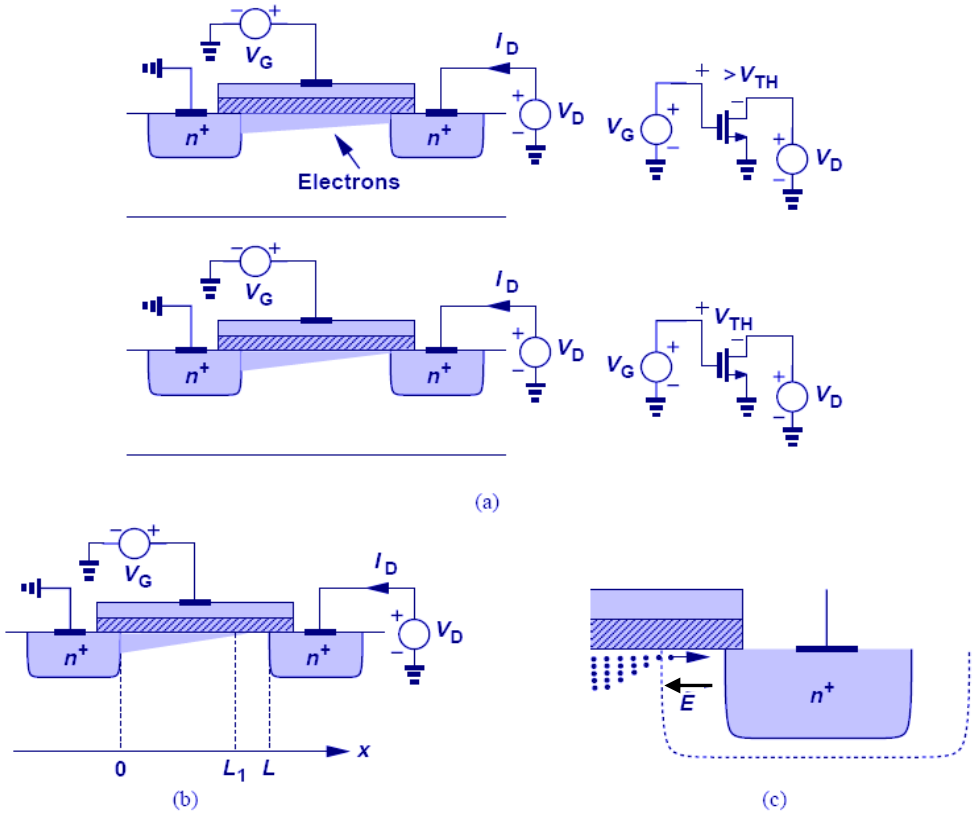
- First, the holes are repelled by the positive gate voltage, leaving behind negative ions and forming a depletion region. Next, electrons are attracted to the interface, creating a channel (“inversion layer”).

Voltage-Dependent Resistor



- The inversion channel of a MOSFET can be seen as a resistor.
- Since the charge density inside the channel depends on the gate voltage, this resistance is also voltage-dependent.

Channel Pinch-Off



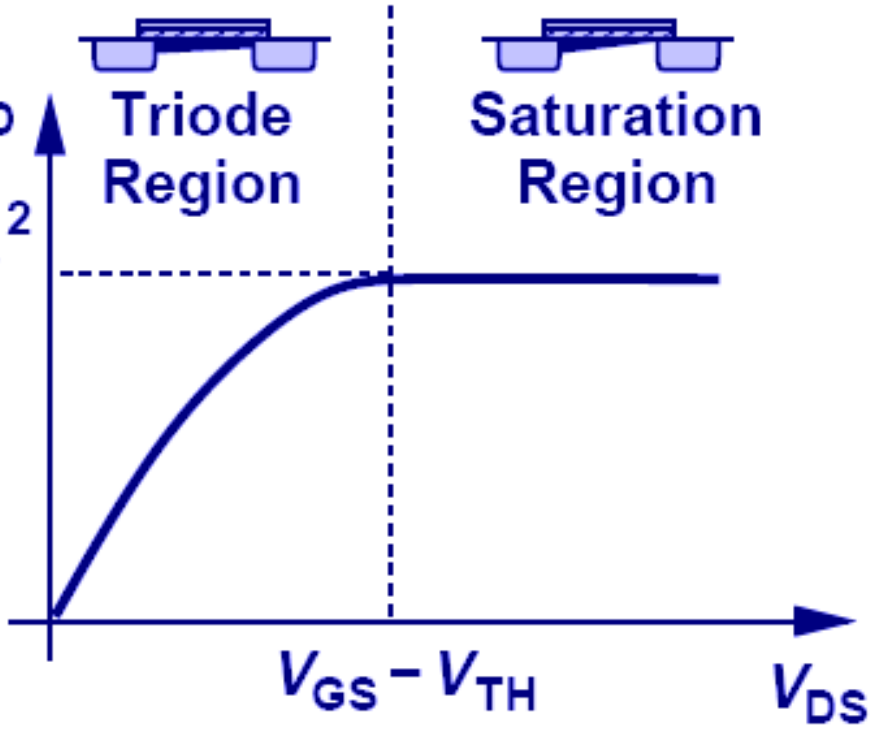
- As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain.
- When $V_D - V_G = V_{th}$, the channel at drain totally pinches off, and when $V_D - V_G > V_{th}$, the channel length starts to decrease.

Different Regions of Operation

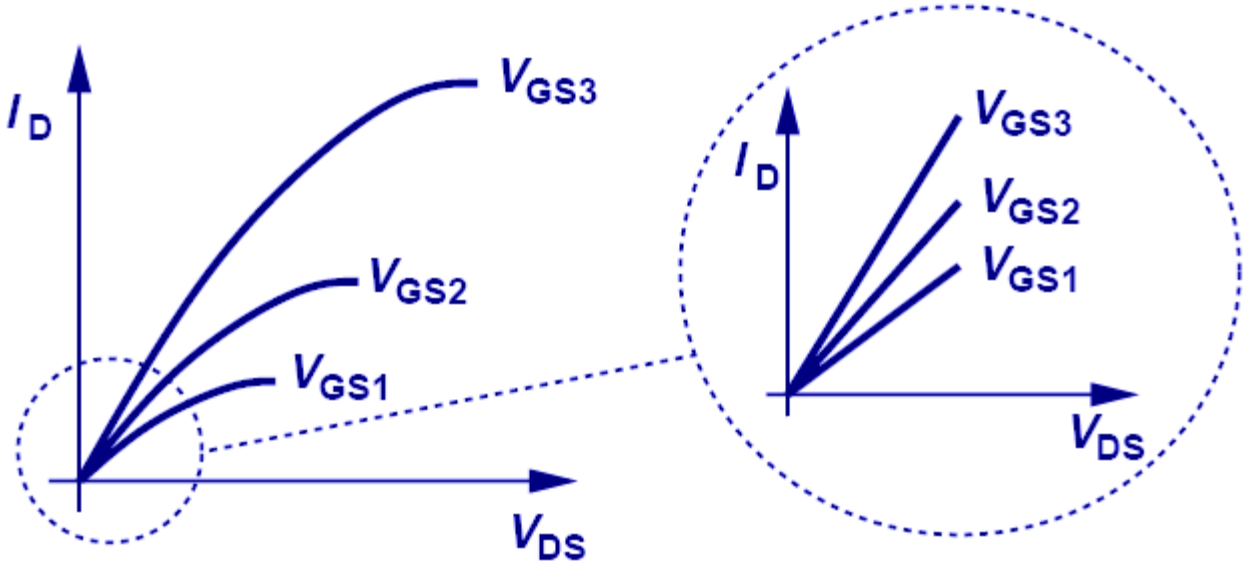
"Triode"

"**Saturation**" or "Pinch off" or "Active" region

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$



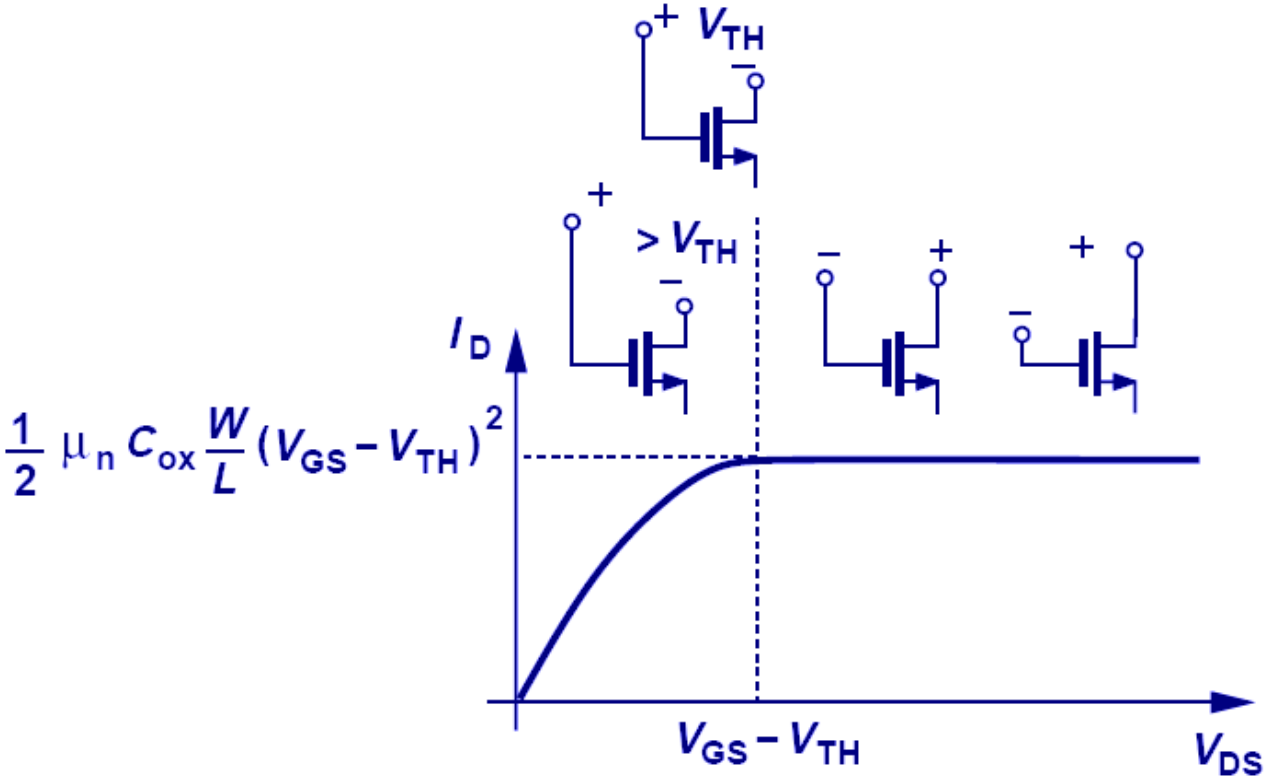
Linear Resistance



$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

- At small V_{DS}, the transistor can be viewed as a resistor, with the resistance depending on the gate voltage.
- It finds application as an electronic switch.

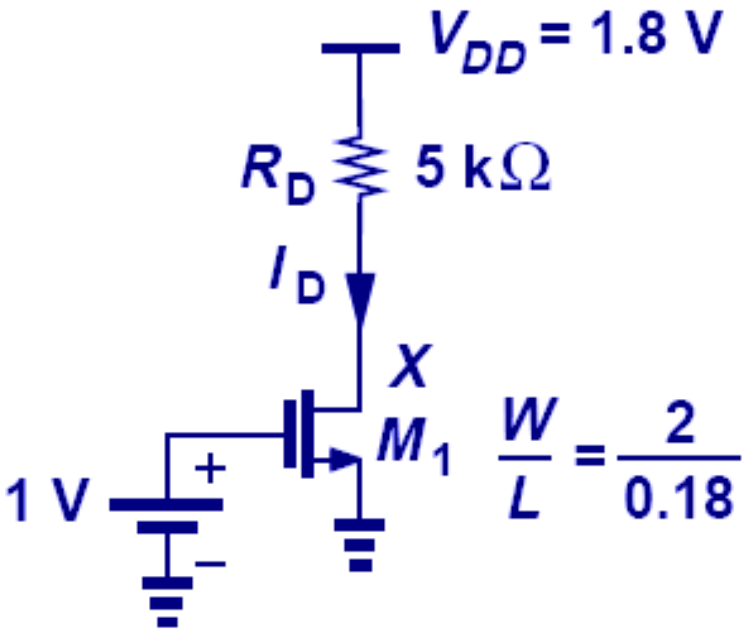
How to Determine ‘Region of Operation’



- When the potential difference between gate and drain is greater than V_{TH}, the MOSFET is in triode region.
- When the potential difference between gate and drain becomes equal to or less than V_{TH}, the MOSFET enters saturation region.

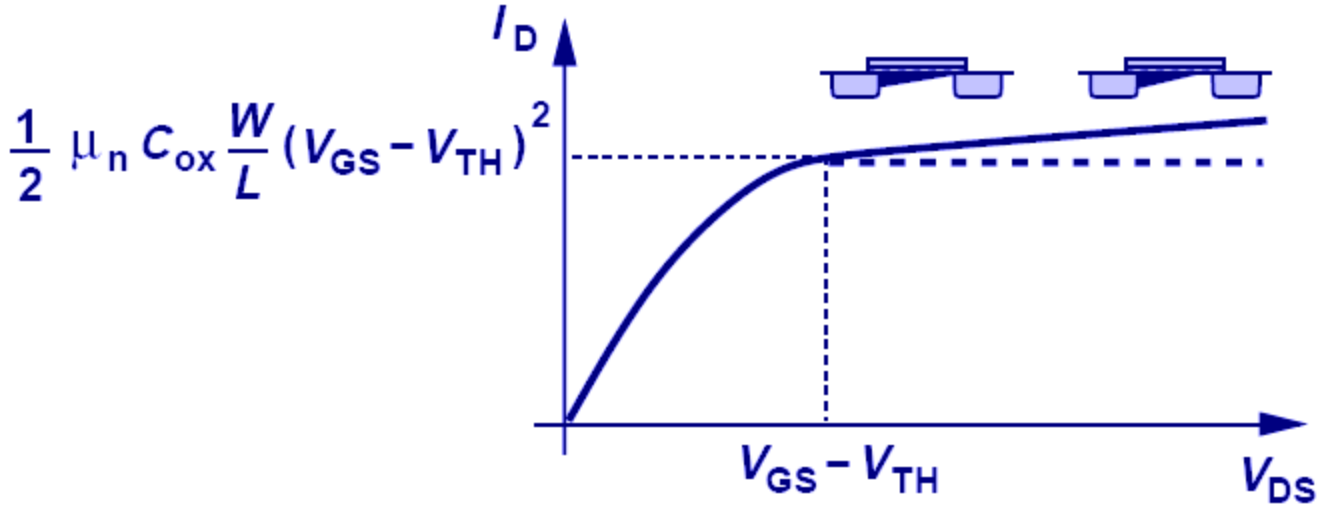
Triode or Saturation?

Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$ and $V_{TH} = 0.4\text{ V}$



- When the region of operation is not known, a region is assumed (with an intelligent guess). Then, the final answer is checked against the assumption.

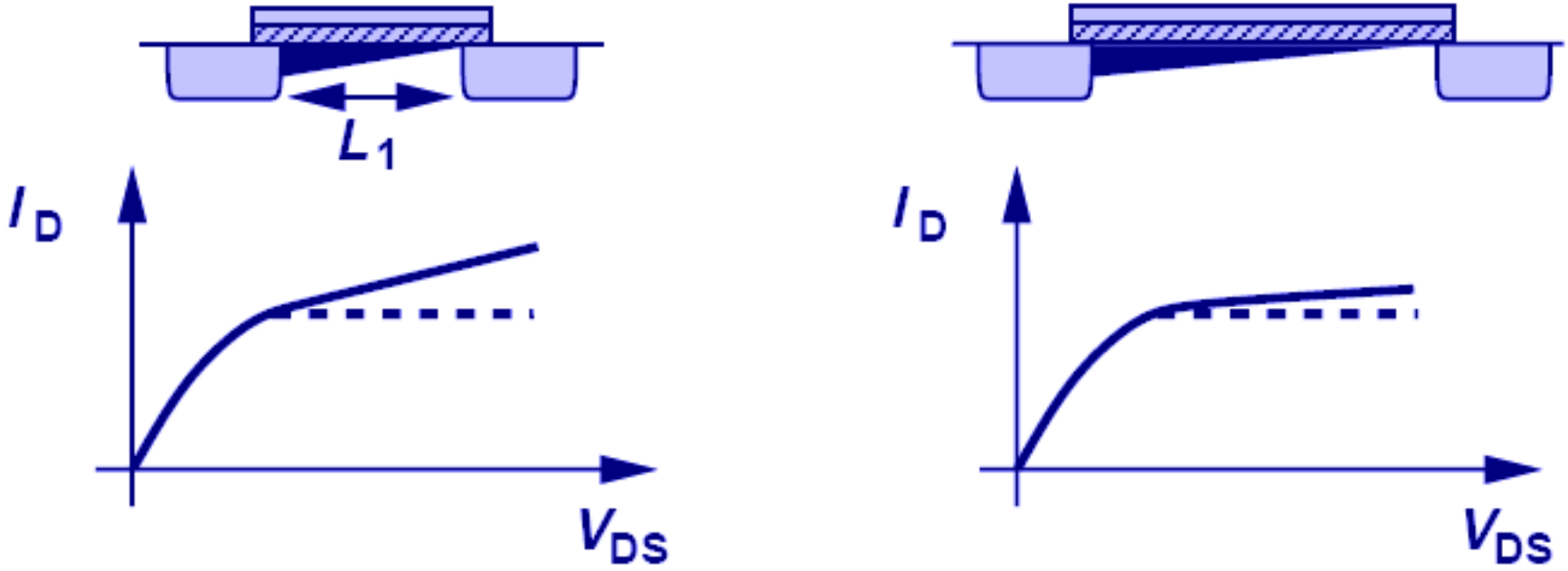
Channel-Length Modulation



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

- The original observation that the current is constant in the saturation region is not quite correct. The end point of the channel actually moves toward the source as V_D increases, increasing I_D. Therefore, the current in the saturation region is a weak function of the drain voltage.

λ and L



- Unlike the Early voltage in BJT, the channel- length modulation factor can be controlled by the circuit designer.
- For long L, the channel-length modulation effect is less than that of short L.

Transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

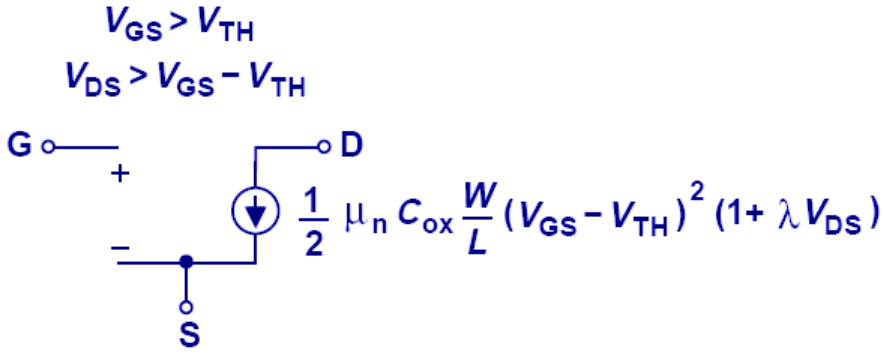
- Transconductance is a measure of how strong the drain current changes when the gate voltage changes

Transconductance

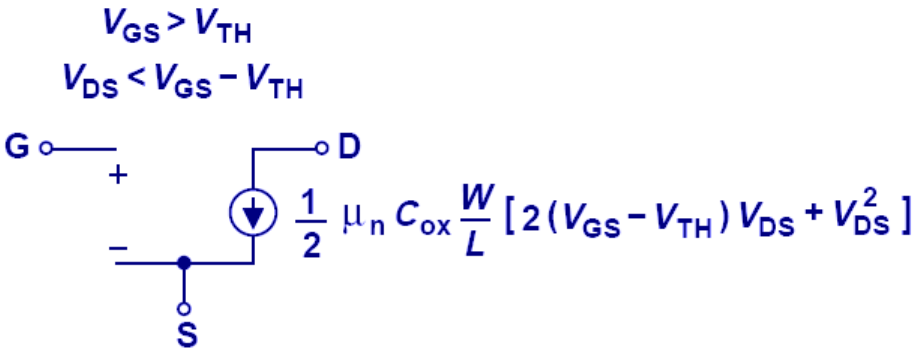
$\frac{W}{L}$ Constant $V_{GS} - V_{TH}$ Variable	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant
$g_m \propto \sqrt{I_D}$ $g_m \propto V_{GS} - V_{TH}$	$g_m \propto I_D$ $g_m \propto \frac{W}{L}$	$g_m \propto \sqrt{\frac{W}{L}}$ $g_m \propto \frac{1}{V_{GS} - V_{TH}}$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \qquad g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \qquad g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

Large-Signal Models



(a)



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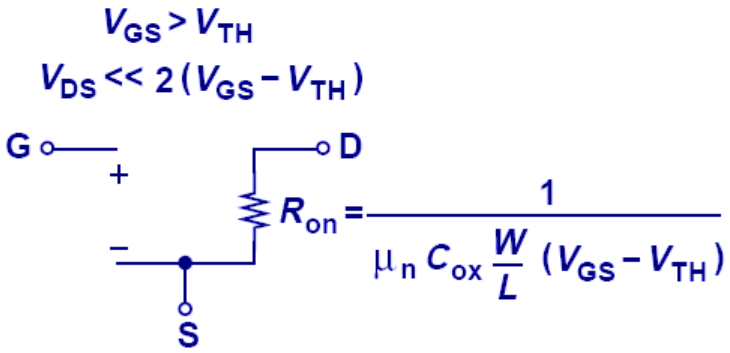
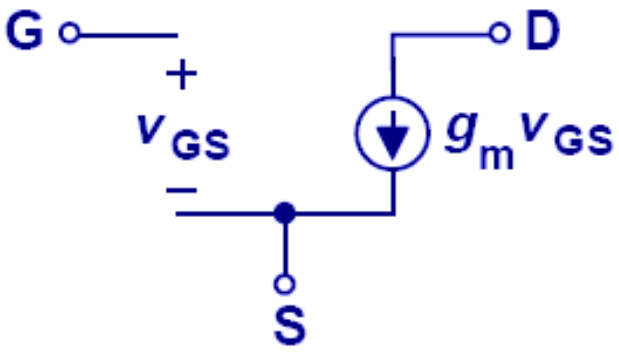


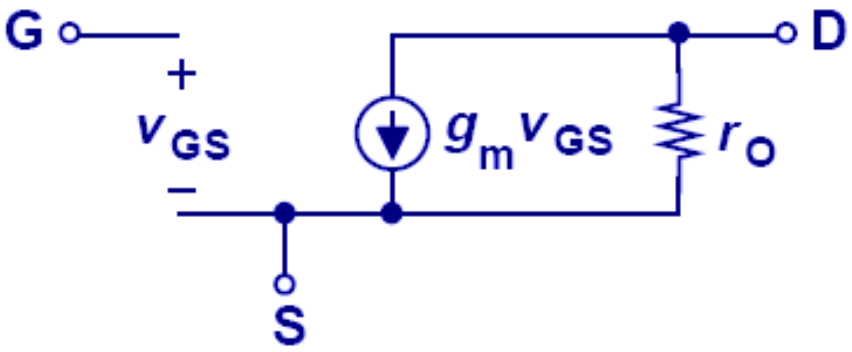
(c)

- Based on the value of $V_{DS,}$ MOSFET can be represented with different large-signal models.

Small-Signal Model



(a)



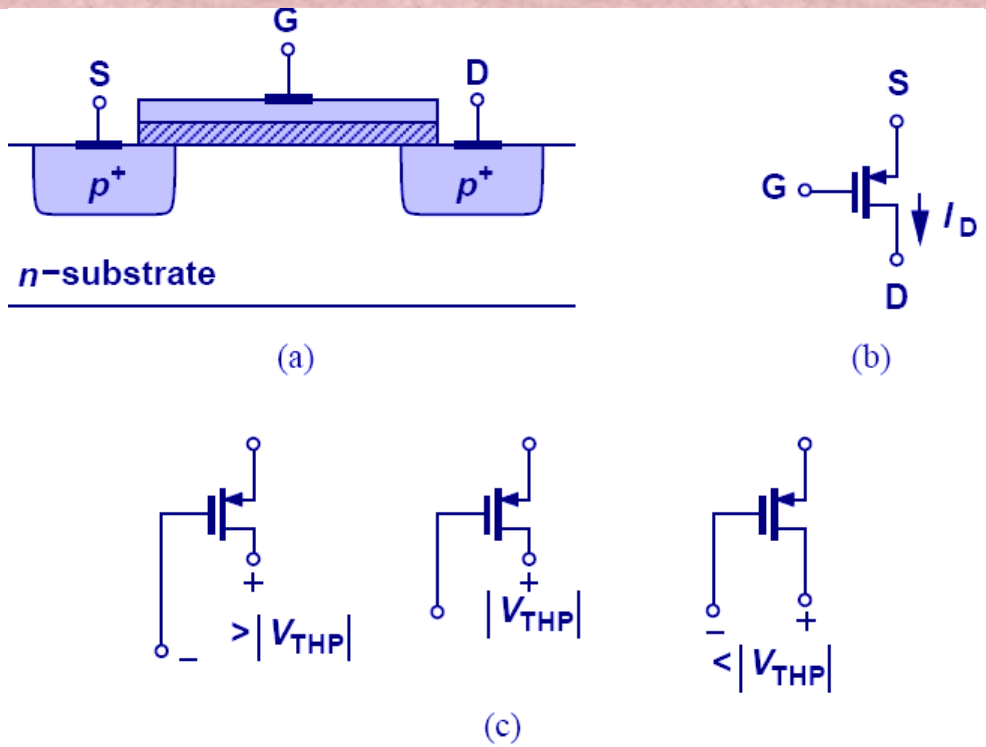
(b)

$$r_o \approx \frac{1}{\lambda I_D}$$

- When the bias point is not perturbed significantly, small-signal model can be used to facilitate calculations.
- To represent channel-length modulation, an output resistance is inserted into the model.

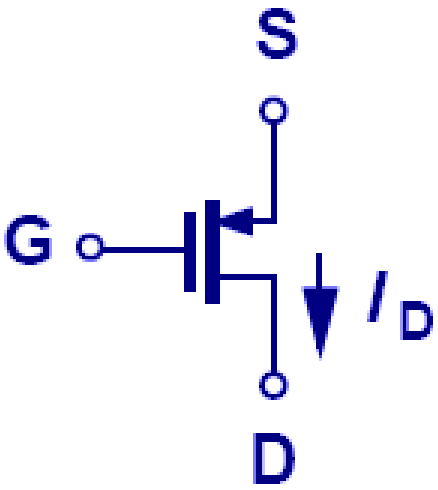
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) \quad \Rightarrow \quad r_o \approx \frac{1}{\lambda I_D}$$

PMOS Transistor



- Just like the PNP transistor in bipolar technology, it is possible to create a MOS device where holes are the dominant carriers. It is called the PMOS transistor.
- It behaves like an NMOS device with all the polarities reversed.

PMOS Equations



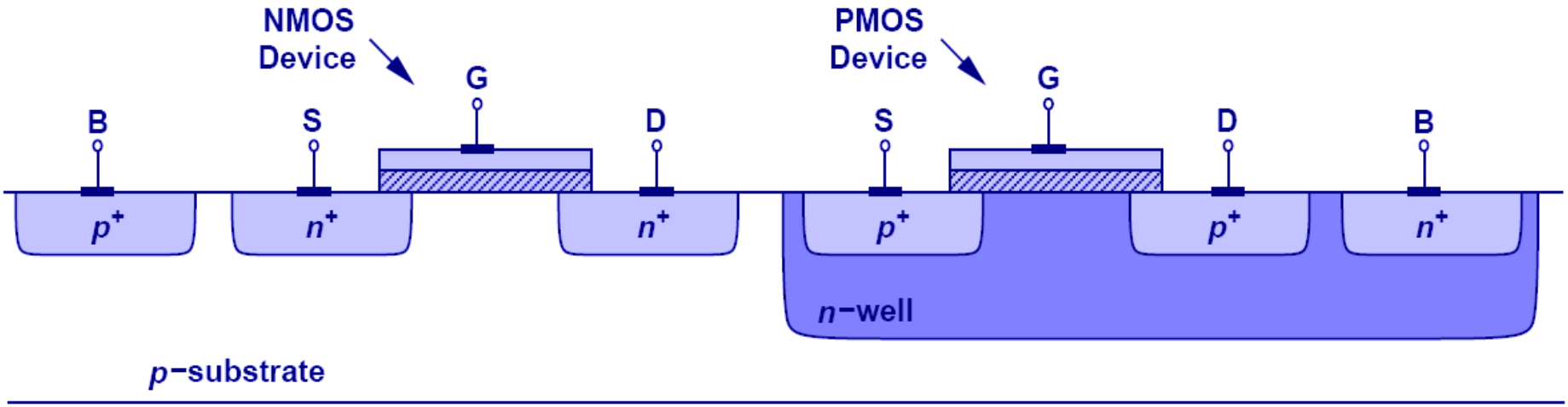
$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$$

$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]$$

$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}| - |V_{TH}|)^2(1 + \lambda|V_{DS}|)$$

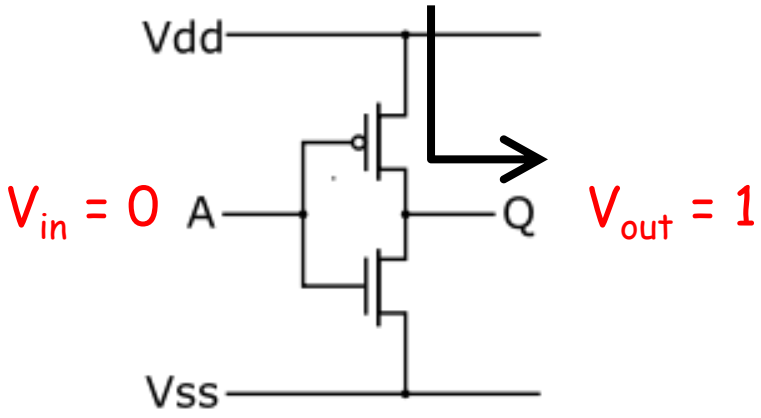
$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(|V_{GS}| - |V_{TH}|)|V_{DS}| - V_{DS}^2\right]$$

CMOS Technology



- It possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.
- It is known as CMOS, or “Complementary MOS”.

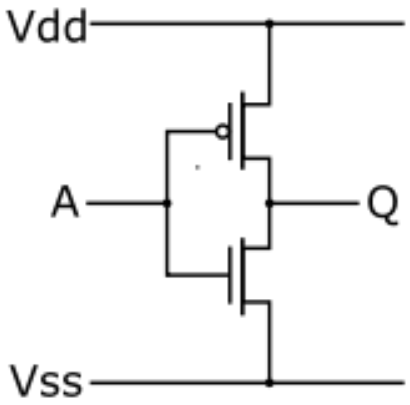
CMOS



NOT gate
(inverter)

Negative gate turns pMOS on

So what?



More importantly, since one is open and one is shut at steady-state, **no current except during turn-on/turn-off**

→ Low power dissipation

Comparison of Bipolar and MOS Transistors

Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel-Length Modulation
Diffusion Current	Drift Current
–	Voltage-Dependent Resistor

- Bipolar devices have a higher g_m than MOSFETs for a given bias current due to its exponential IV characteristics.