UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
ECE (8101) 432
Object Oriented Modeling of Electronic Circuits – Spring 97-98
Midterm Exam

Computer Account#_____

First Name:_____

Last Name:_____

Student Number:_____

Signature:_____

Grade:

Problem 1. _____/20

Problem 2. _____/25

Problem 3. _____/25

Problem 4. _____/30

Total: _____/100

Copper work, Zanjan, Iran. Aban 1397.

DO NOT USE LAPTOPS
EXTRA SHEETS WILL NOT BE ACCEPTED
YOU MUST SHOW COMPLETE WORK ON ALL PROBLEMS
YOU HAVE EXACTLY 150 MINUTES FOR WORKING ON THIS TEST
THIS IS AN OPEN NOTE EXAM, NO SHARING ALLOWED

C/C++ Logic Modeling

1. Using functions developed in C++ for logic modeling, write a C++ model for an ABS(x) circuit. The absolute value circuit receives an 8-bit two's complement data. The 8-bit output of circuit is the absolute value of the input data. Use combinational components discussed in class.

C/C++ RTL Components

2. Using the *bus* class components, overloaded operations, and other utilities, show the description of an 8-bit shift register with bidirectional input output lines using *oe*, right-shift using *si*, and parallel load using *ld*. Inherit this class from the *dRegister* class discussed in class. Provide a resetting mechanism and use clocking scheme used in conjunction with the *bus* library.

C++ Bus Library Controller

3. Show the design of a circuit that finds the remainder of 3 of the sum of all synchronous 2-bit numbers received over its 2-bit input *A*. show the state diagram and the C++ implementation of this circuit using the *bus* class discussed in class.

SystemC Component and test

4. Show SystemC description at the RT level for a maximum finder sequential circuit that finds the maximum positive number among the sequence of 8-bit input data, received on its *inBus*, starting from a positive pulse on input *start* and ending with a positive pulse on input *end*. The circuit is in *Idle* mode with its *ready* signal asserted until its input *start* becomes one. After this, when *start* becomes zero, on each positive edge of the clock, the circuit receives an 8-bit input and compares it with the pervious inputs it has received and keeps the largest of the data received. When the *end* signal is issued, search for data in *inbus* ends, and the largest data receiving becomes available on the *outBus* and the *ready* signal will be issued.
    a. Show the datapath and controller for this circuit and the wiring signals between them.
    b. Write SystemC description for the circuit and provide an appropriate testbench.
    c. Show the simulation environment using *sc_main*.