UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
ECE (8101) 432

Object Oriented Modeling of Electronic Circuits – Spring 96-97
Midterm Exam

Computer Account#_____

First Name:_____

Last Name:_____

Student Number:_____

Signature:_____

Grade:

Problem 1. _____/25

Problem 2. _____/25

Problem 3. _____/25

Problem 4. _____/25

Total: _____/100

Ghale Rood-khaan, Rood-Khan, near Fooman, Guilan, Iran

DO NOT USE LAPTOPS
EXTRA SHEETS WILL NOT BE ACCEPTED
YOU MUST SHOW COMPLETE WORK ON ALL PROBLEMS
YOU HAVE EXACTLY 150 MINUTES FOR WORKING ON THIS TEST
THIS IS AN OPEN NOTE EXAM, NO SHARING ALLOWED

C/C++ RTL Modeling

1. In the *bus* class developed for RTL modeling, various operations are overloaded that operands of the *bus* class can use. To this library, add the overloading of the >> operation that shifts to the right its *bus* type (left) operand by the number of bits of the integer right operand, e.g., *xbus >> 5*. The result is a *bus* vector of the same size of the left operand. Empty bits on the left of the result become zero.

C/C++ RTL Components

2. Using the *bus* class components, overloaded operations, and other utilities, show the design of a circuit that is continuously receiving 8-bit parallel data and showing the maximum of all data ever received. Provide a resetting mechanism and use clocking used in conjunction with the *bus* library.

SystemC Controller

3. A controller is to be designed to control shifting of serial data into an n-bit shift register. This situation happens when shifting serial scan data into the register part of a circuit for testing. Shifting begins after *shiftBegin* becomes 1. Shifting continues for 432 clock cycles and with every shift, serial data is shifted into the scan register (you need not be concerned with the scan part). When 432 is counted, the controller issues *shiftEnded* signal for one clock cycle. Show a block diagram of this controller including its state machine and its counter. Write SystemC description of these two part and instantiate them both in a SystemC module called *shiftController*.

SystemC Component and test

4. Show SystemC description for a 16-it register complex with a rising edge clock and an asynchronous active high reset. The register complex has a 2-bit *mode* input based on which the following operations are performed: 00: Do nothing, 01: Count up, 10: Swap right and left bytes, and 11: Parallel load. Write complete SystemC description, a testbench, and show how the testbench is instantiated in an *sc_main*.