UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

ECE (8101) 432

Object Oriented Modeling of Electronic Circuits – Spring 94-95

Midterm Exam

Computer Account#_______________________

First Name:_______________________________

Last Name:_______________________________

Student Number:_________________________

Signature:________________________________

Grade:

Problem 1. ______	/25
Problem 2. ______	/25
Problem 3. ______	/25
Problem 4. ______	/25
Total: ______	/100

Sanandaj, Kurdistan, Iran

DO NOT USE LAPTOPS
EXTRA SHEETS WILL NOT BE ACCEPTED
YOU MUST SHOW COMPLETE WORK ON ALL PROBLEMS
YOU HAVE EXACTLY 150 MINUTES FOR WORKING ON THIS TEST
THIS IS AN OPEN BOOK OPEN NOTE EXAM, NO SHARING ALLOWED

C/C++ Gate Level Classes

1. Write a C++ NAND model that will not require ordering when used in a combinational circuit. Use the base model from gates discussed in class, and add an event field to it. Gates will be used in a loop and iteration through the loop continues until no gate in the loop has had a fresh event in its event field.
   - A) Write event based NAND gate.
   - B) Show a FA using NAND gates.
   - C) Use gates of the FA in an event based loop for unordered implementation of the full-adder.

C/C++ RTL Components

2. **A)** Write a C++ class description for an 8-bit *baseCounter* with parallel load (*ld*), count-up enable (*ce*), carry-in (*ci*), clock (*clk*), asynchronous reset (*rst*), and a carry-out (*co*). Write an *evl* function that performs the count function. For inputs and outputs use wire pointers. Use the *bus* class for all signals. **B)** Inherit from the counter of Part A the *nCounter* counter that adds a parallel *nCount* input and an *init* input to the *baseCounter* class. After a synchronous 1 on *init*, the *nCounter* initializes to count *nCount* clocks before it issues a pulse on *reached*.

C/C++ Controller

3. Show C++ description of a Mealy sequence detector that detects the 110 sequence on its *a* input. Use Huffman coding style.

C/C++ RT Level Design Coding

4. In this assignment you are to design an RT level circuit that finds the maximum of *n* data words and places the result on the output. The circuit is called N Max Finder (NMF). After a complete pulse on *start*, the circuit starts its processing and when completed, the largest of all data received will be placed on the 8-bit *largeBus*. At this time the circuit asserts the *done* signal, which will remain asserted until the next round of input data begins. Input data arrive via the 8-bit *inputBus*. After the start, the first data on *inputBus* is the number of data (*n*) that will be arriving on the next *n* clock pulses via this bus. The next *n* clocks each bring in one 8-bit data, the maximum of which is to be calculated.

   A) Show the complete datapath of this circuit

   B) Clearly show control signals from the datapath to the control-unit and back

   C) Show the circuit controller using a state machine

   D) Develop the complete controller (CU) using C++ and the library discussed in class

   E) Implement the datapath (DP) of the circuit using *bus* based components and utilities discussed in class and the *nCounter* of Problem 2

   F) Complete the design of NMF by wiring CU and DP in a top-level testbench that properly orders the datapath and controller