

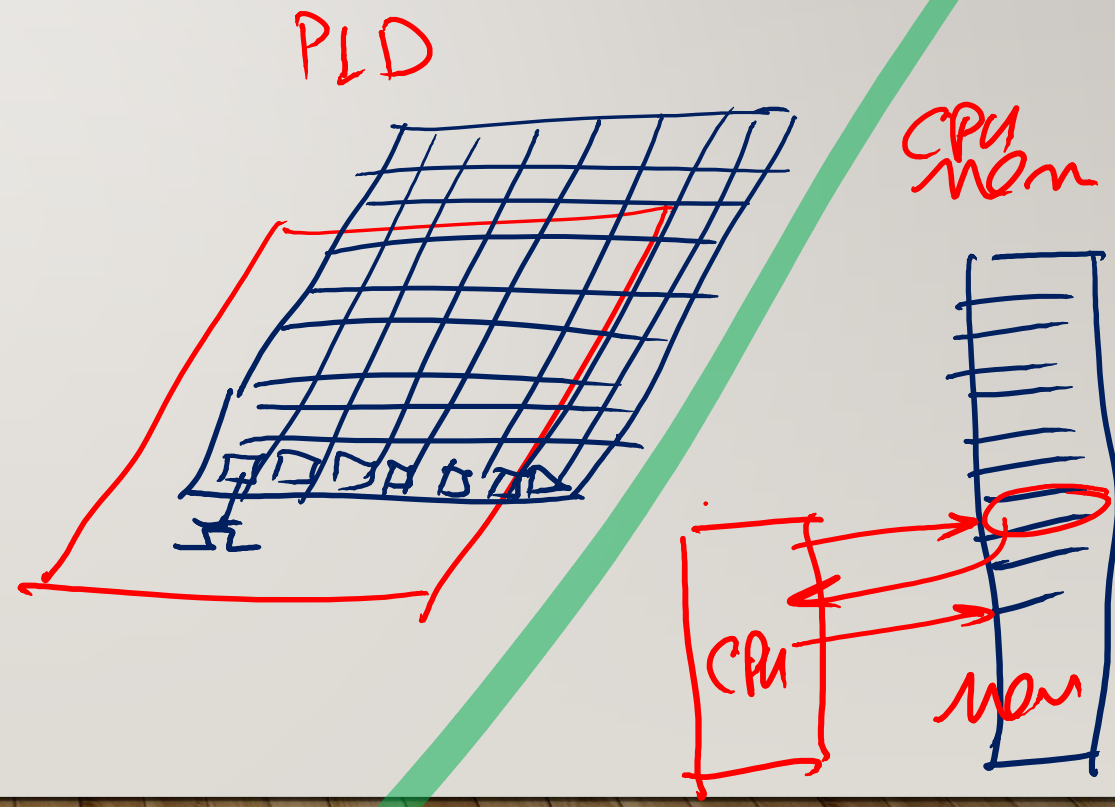
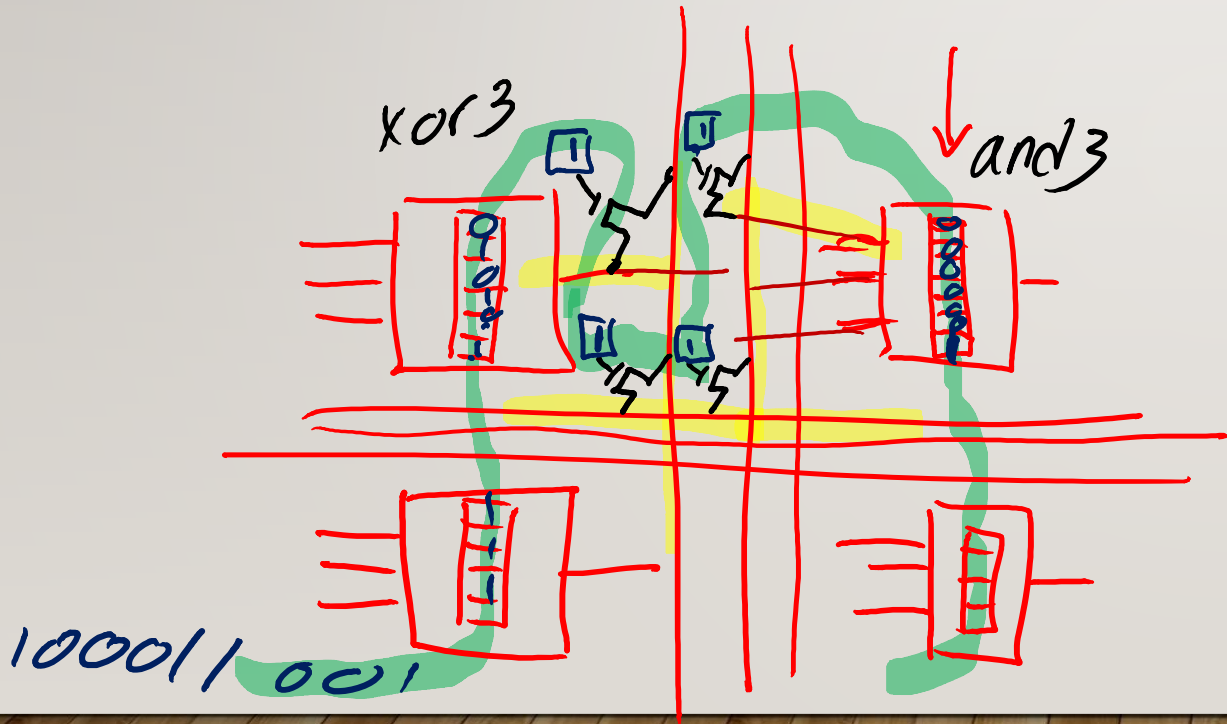


# Digital Logic Design

## Lecture 10

**Dr. Navabi**

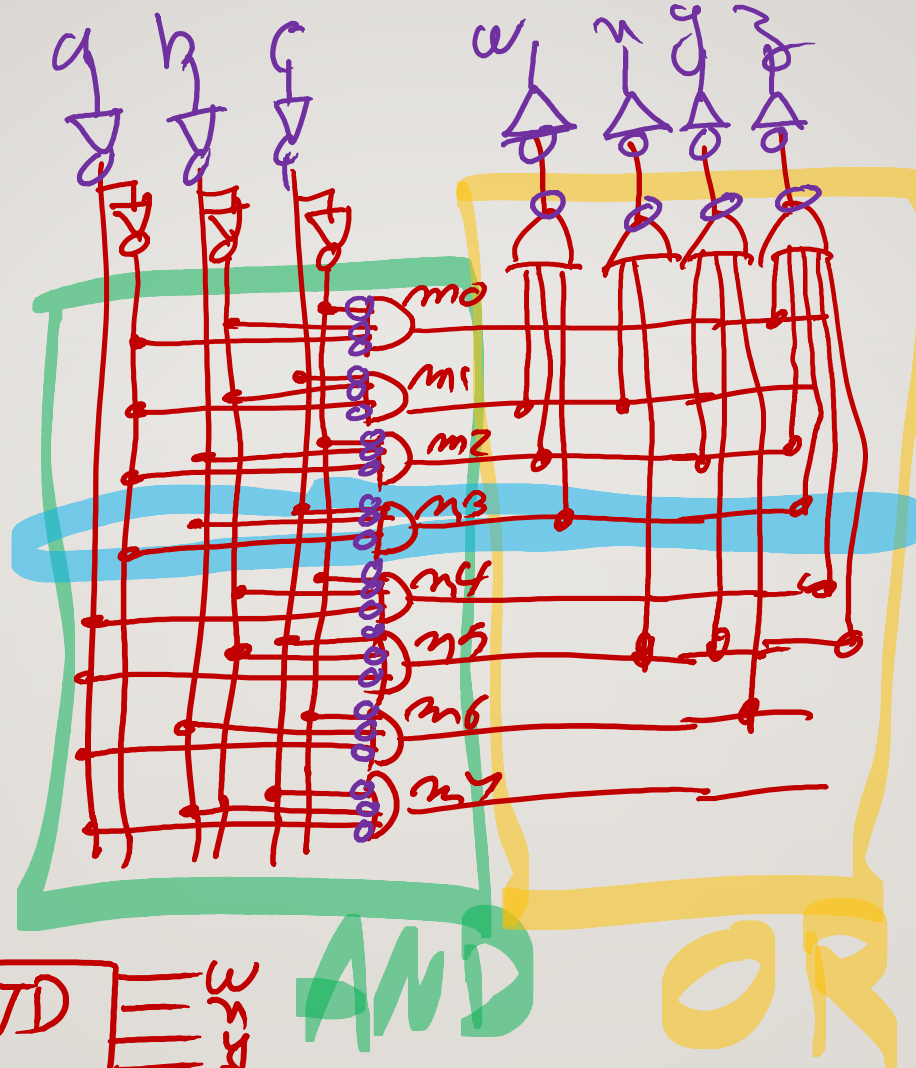
# 2 PLDs Prog. Logic Devices



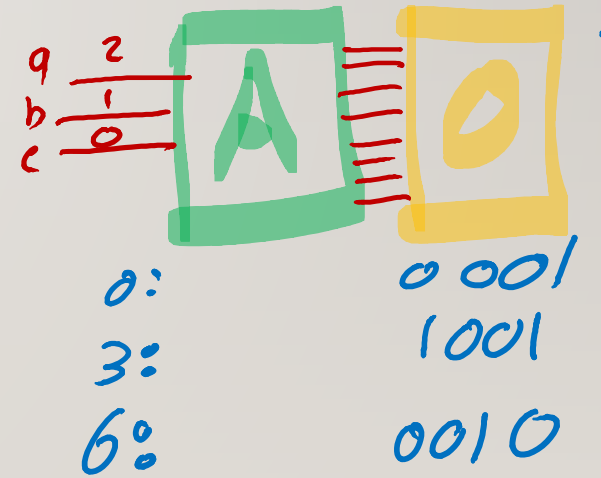
3

PLD

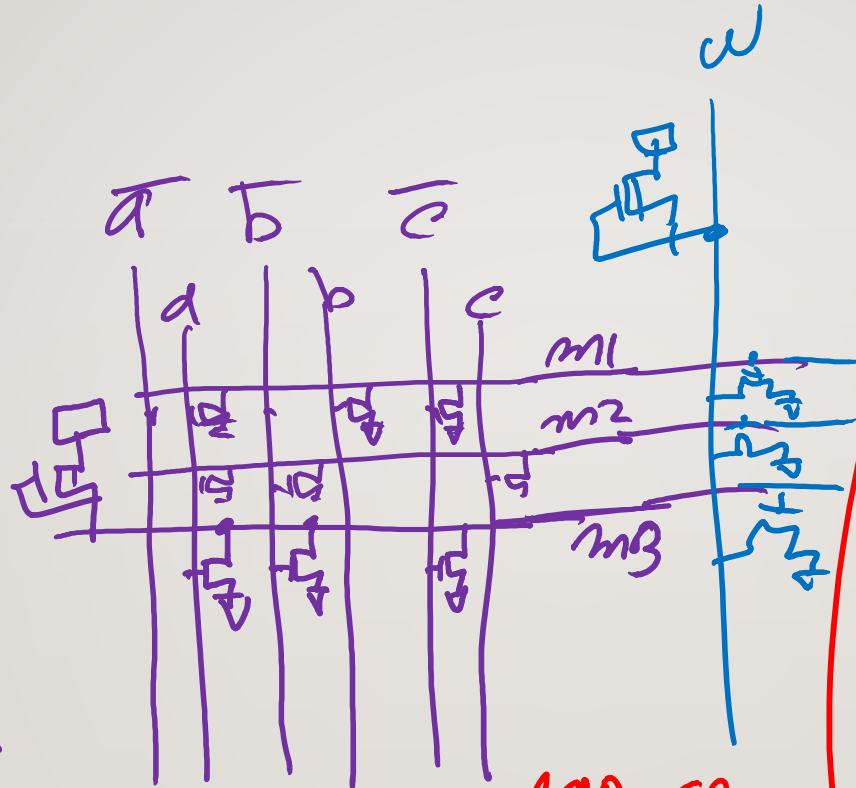
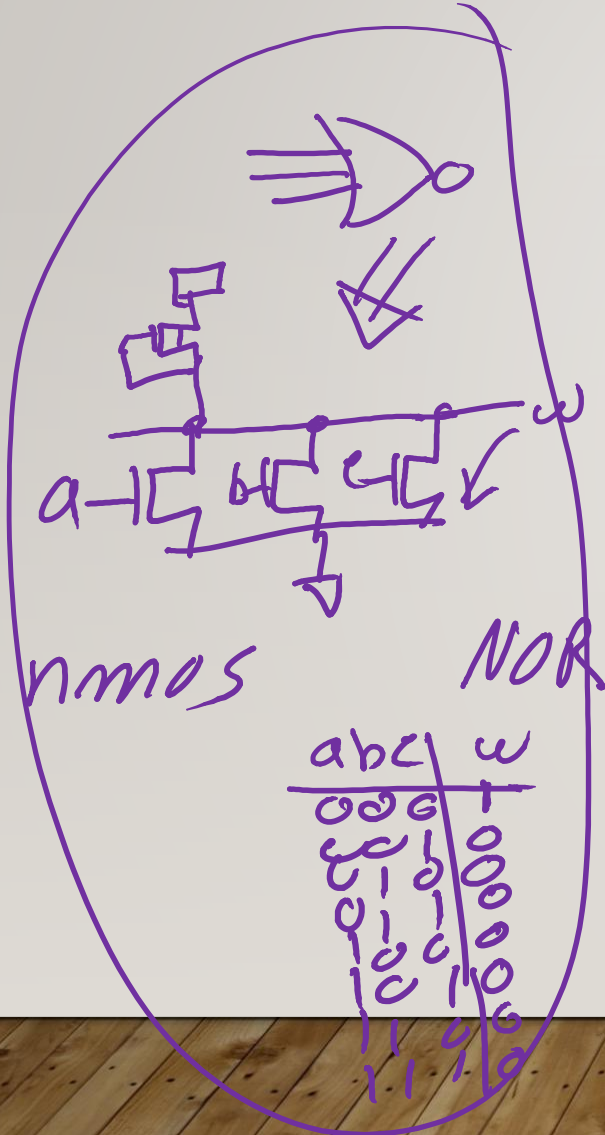
	a	b	c	w	x	y	z
0	0	0	0	0	0	0	1
1	0	0	1	1	1	0	0
2	0	1	0	1	0	1	1
3	0	1	1	0	0	0	1
4	1	0	0	0	0	0	1
5	1	0	1	0	1	1	1
6	1	1	0	0	0	1	0
7	1	1	1	0	0	0	0



ROM  
read only Mem



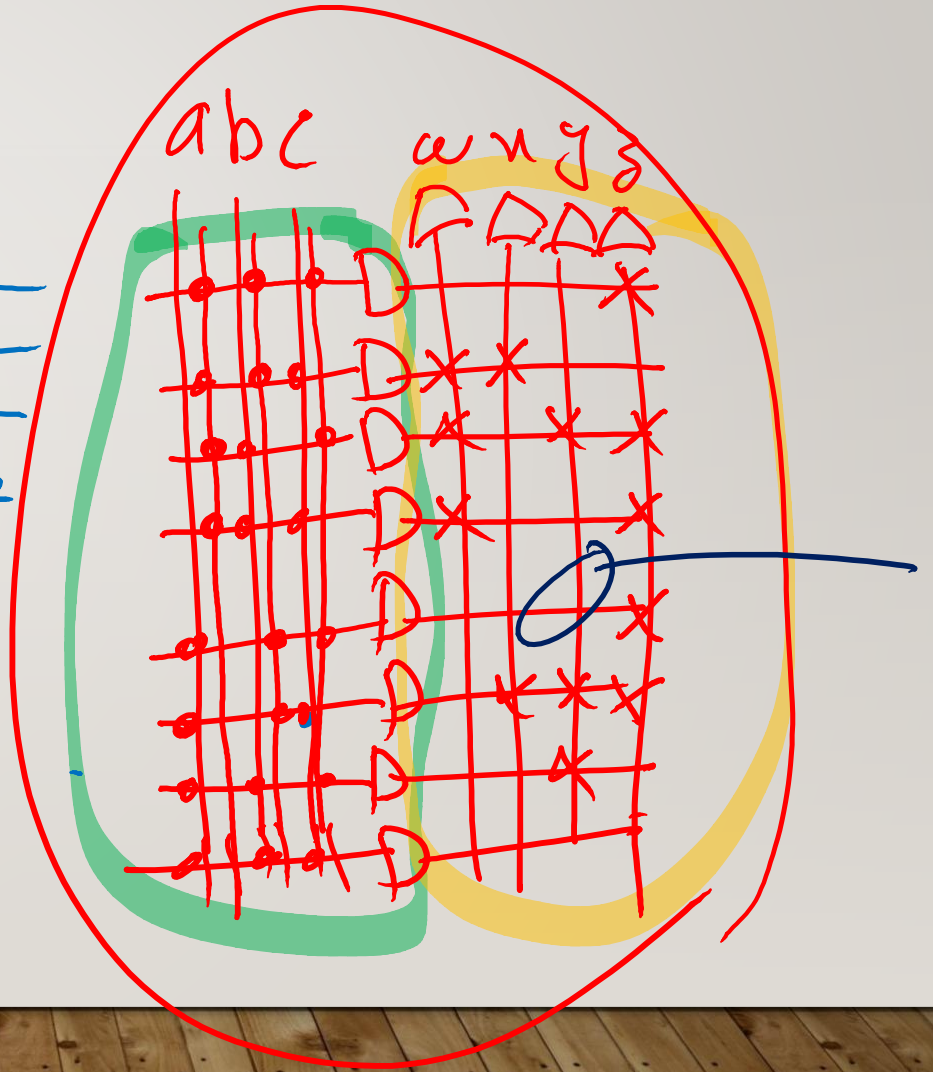
4



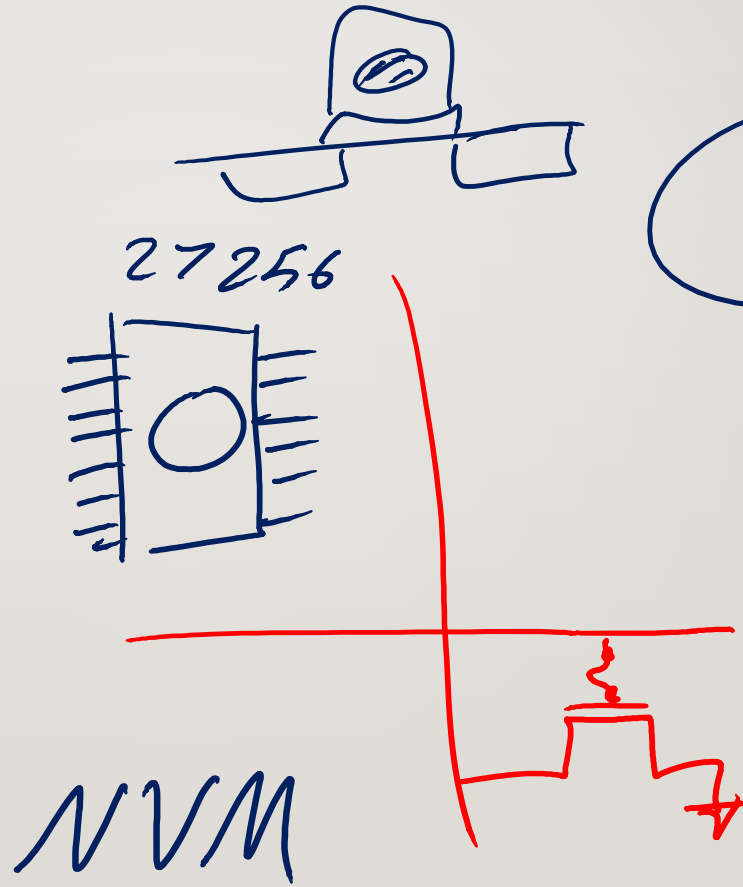
ROM

AND OR

F	P.
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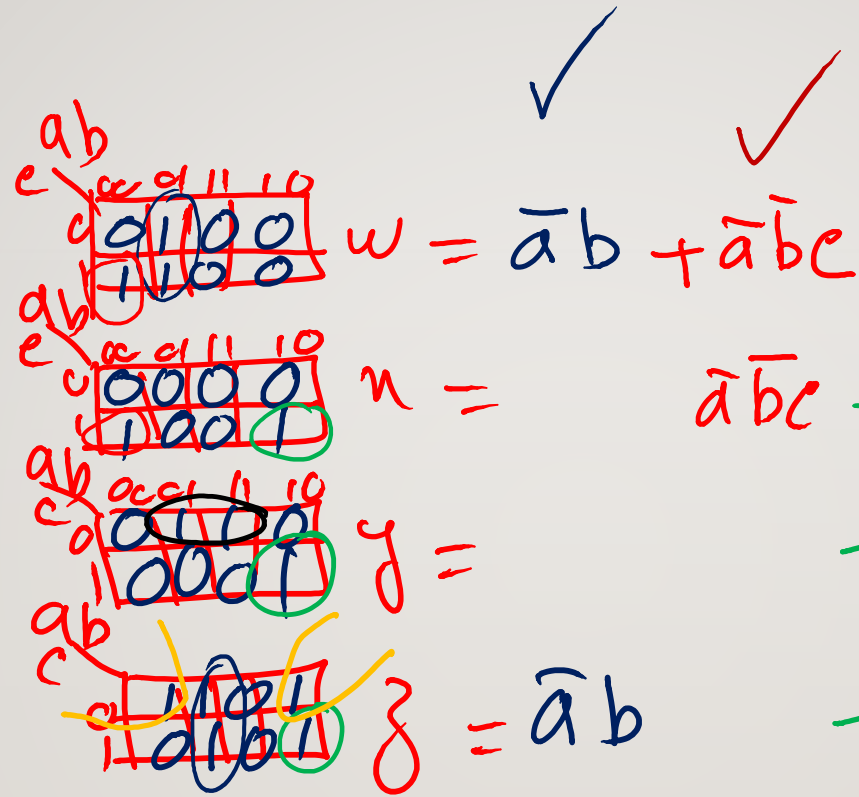
5



- ROM
- PROM
- EPROM
- EEPROM
- Flash

6

a	b	c	w	x	y	z
0	0	0	0	0	0	1
0	0	1	1	1	0	0
0	1	0	1	0	1	1
0	1	1	1	0	0	1
1	0	0	0	0	0	1
1	0	1	0	1	1	1
1	1	0	0	0	1	0
1	1	1	0	0	0	0



PLA



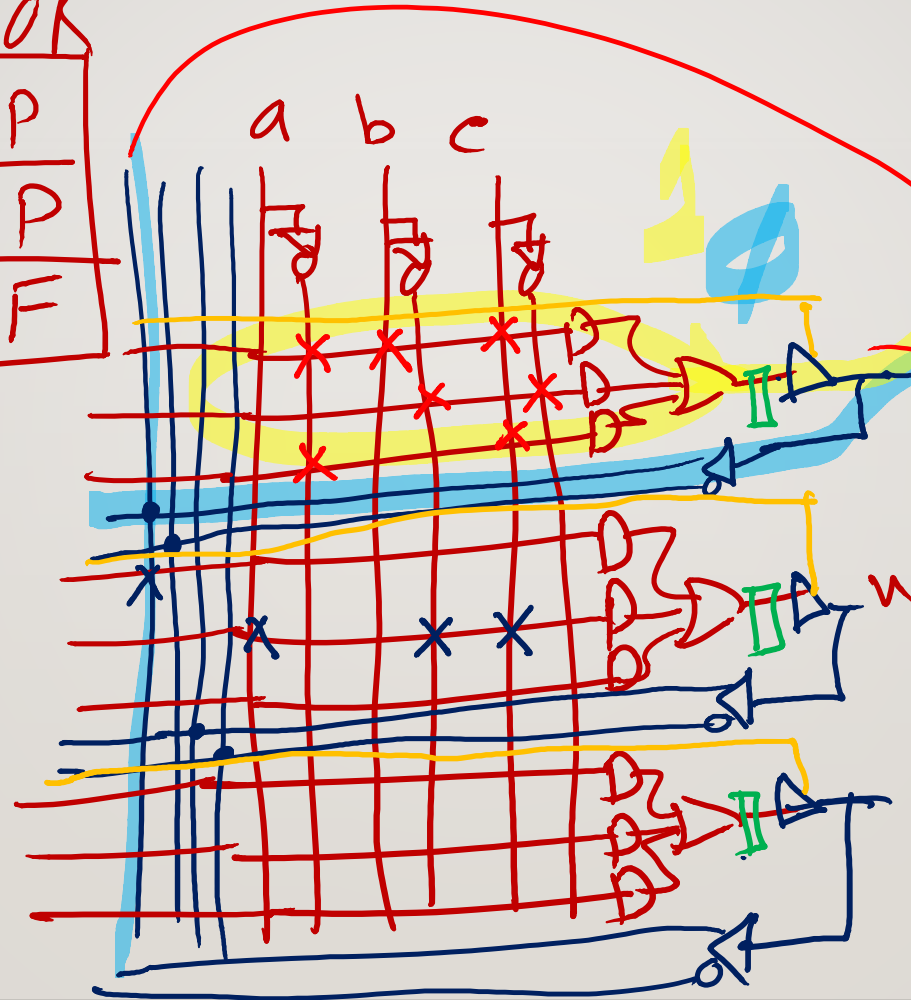
7

	AND	OR
ROM	F	P
PLA	P	P
PAL	P	F

MONOLITHIC memories

PALASM

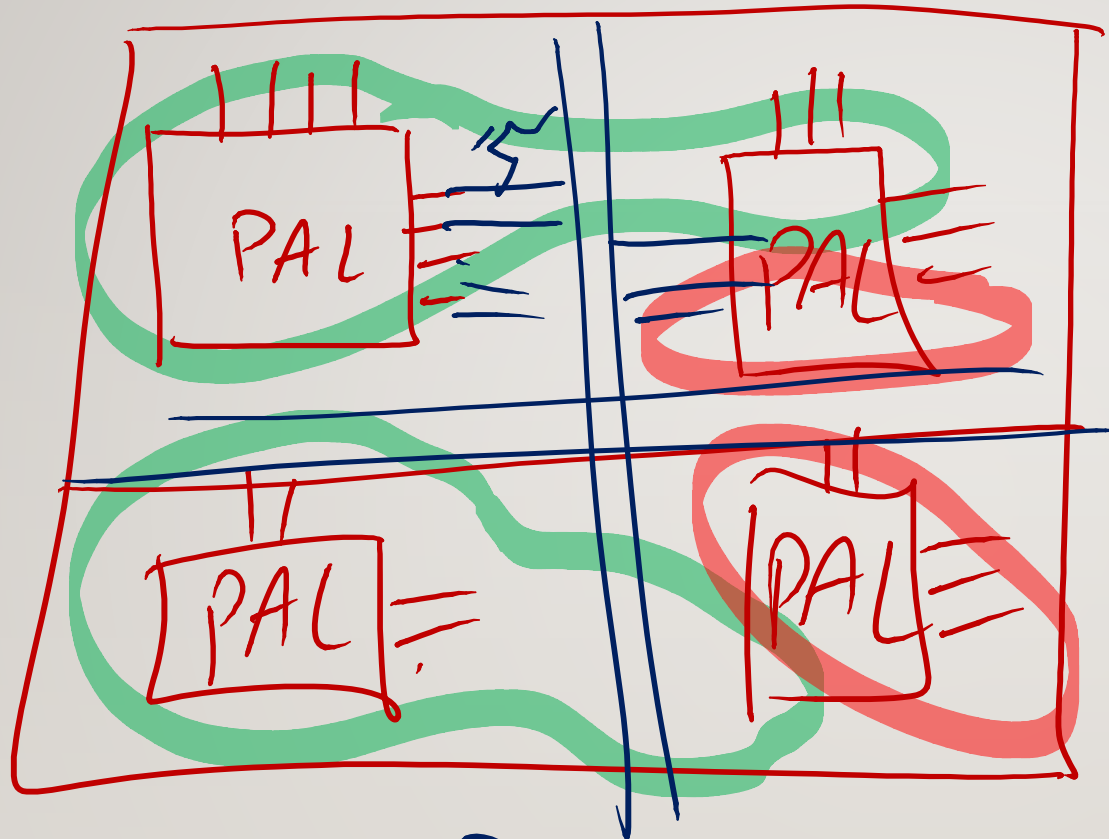
PAL



$$v = \bar{a}bc + b\bar{c} + a\bar{c} + \bar{b}ca$$

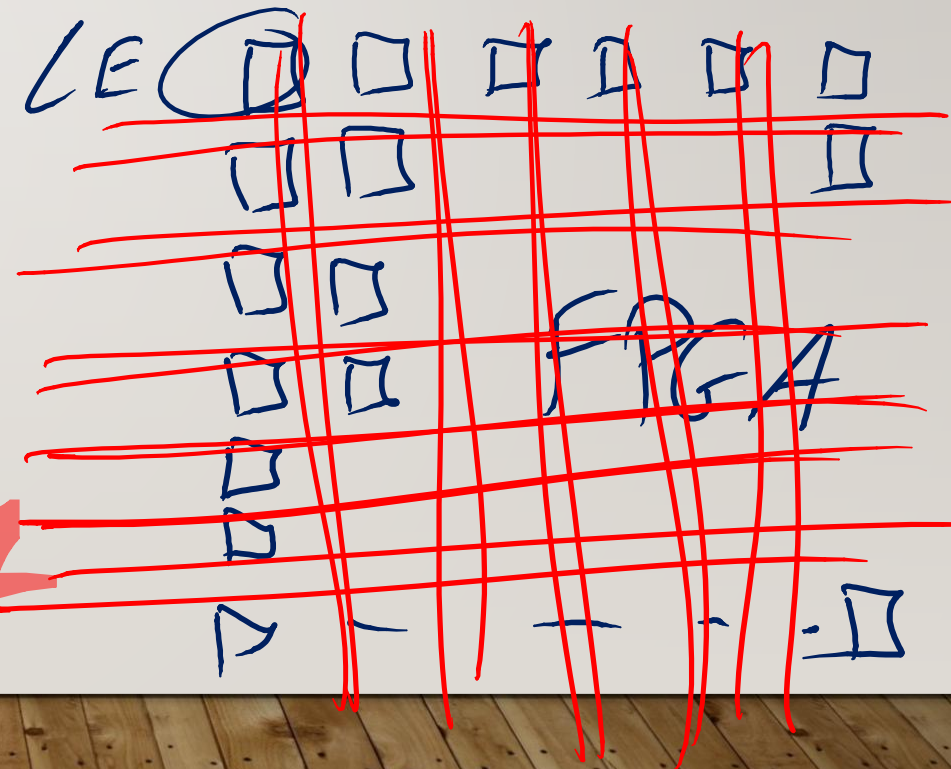
PLDd Term ex.

8



CPLD

Verilog





9

LF  
LB

