ICEEP
Iran Center of ESL Education and Promotion

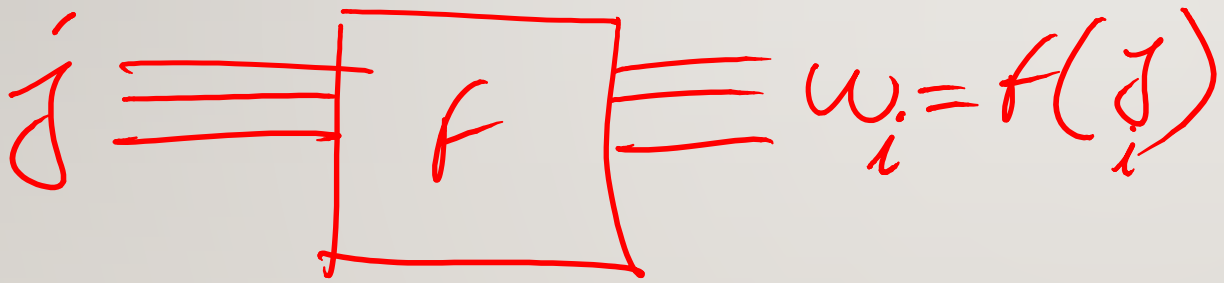
# Digital Logic Design

## Lecture 7

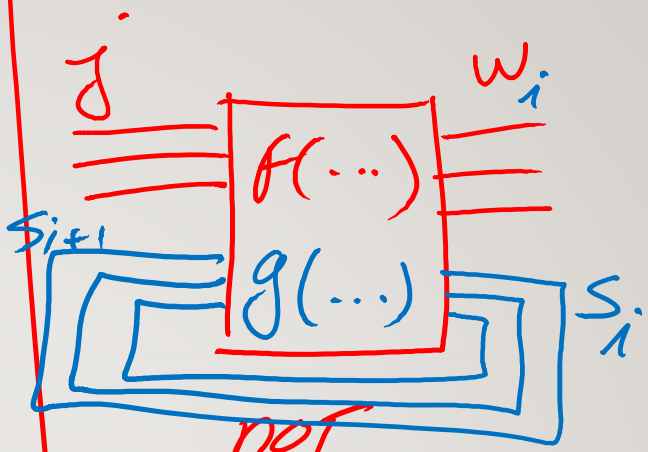
**Dr. Navabi**

# Lecture 7

## Memory




Combinational




not

$w_i \neq f(j_i)$

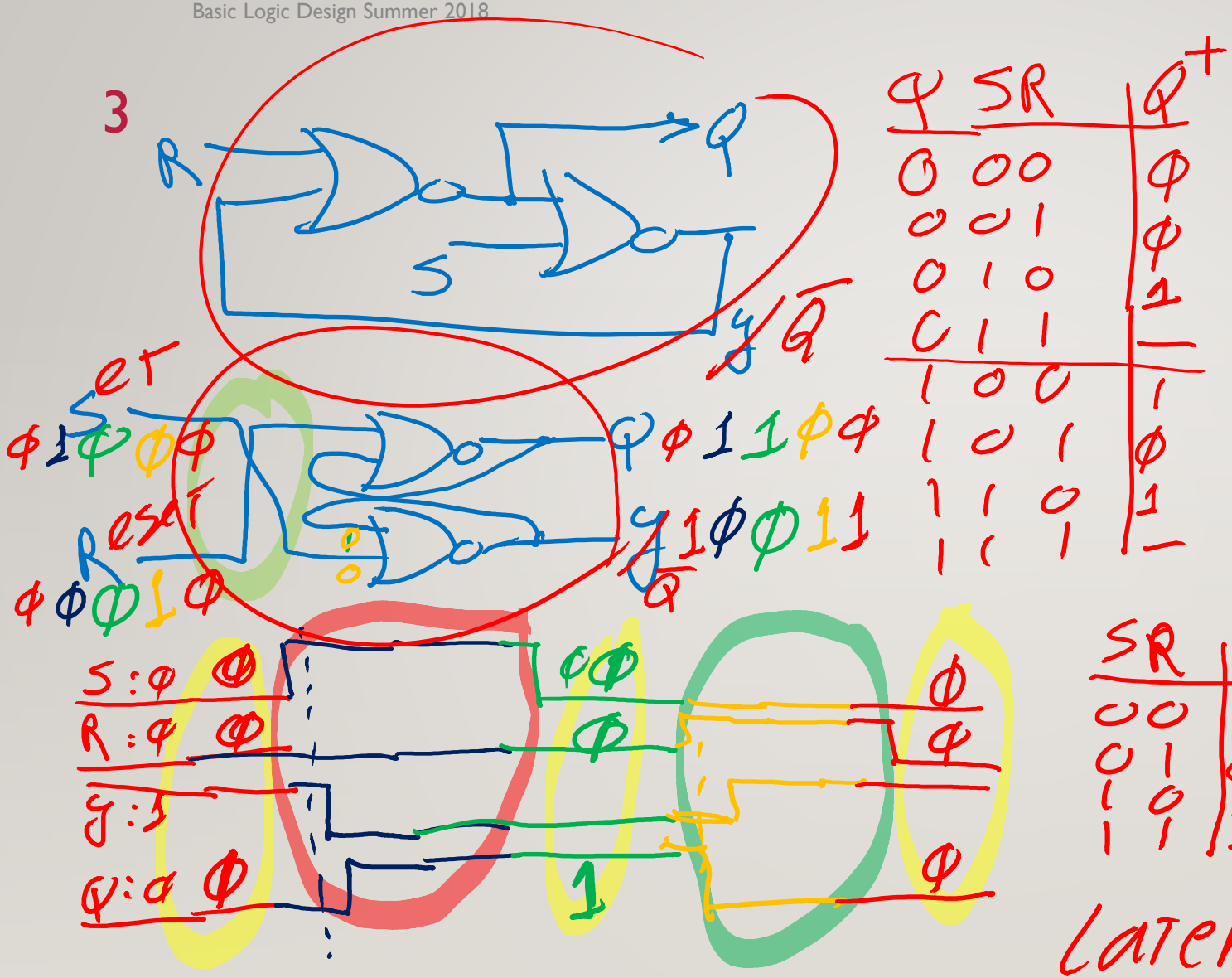
$w_i = f(j_i, j_{i-1}, j_{i-2}, \ldots)$

$w_i = f(j_i, s_i)$

$s_{i+1} = g(j_i, s_i)$

Sequential ckt

3



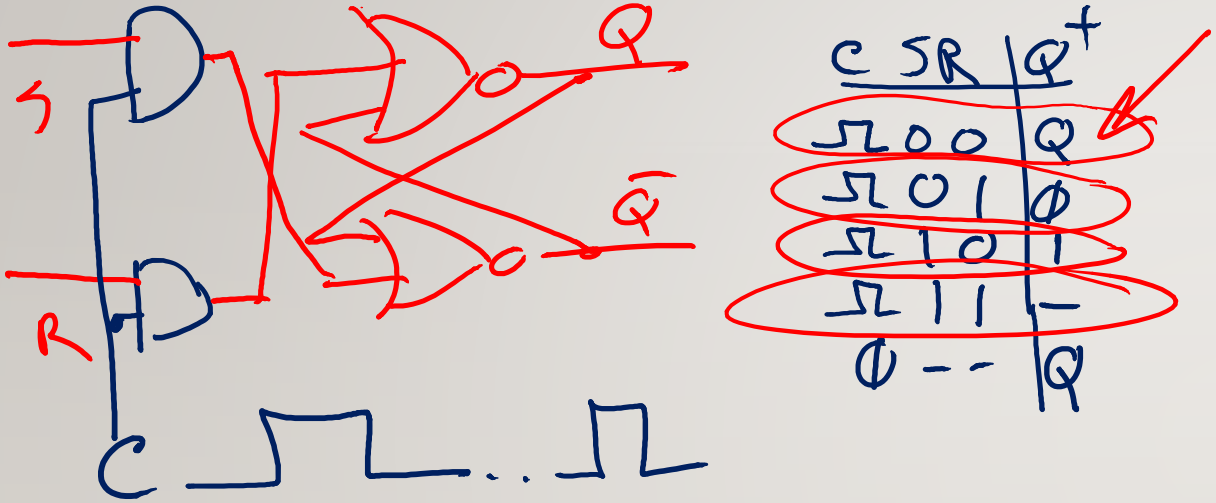

| Q | S | R | $Q^+$ |
|---|---|---|---|
| 0 | 0 | 0 | Q |
| 0 | 0 | 1 | Q |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | — |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | — |

| S | R | $Q^+$ |
|---|---|---|
| 0 | 0 | Q |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | — |

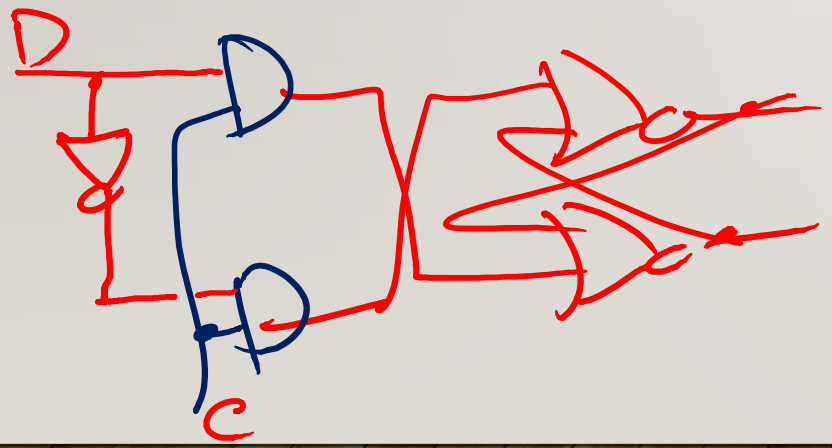
Cross-coupled NOR

Latch, SR

# 4



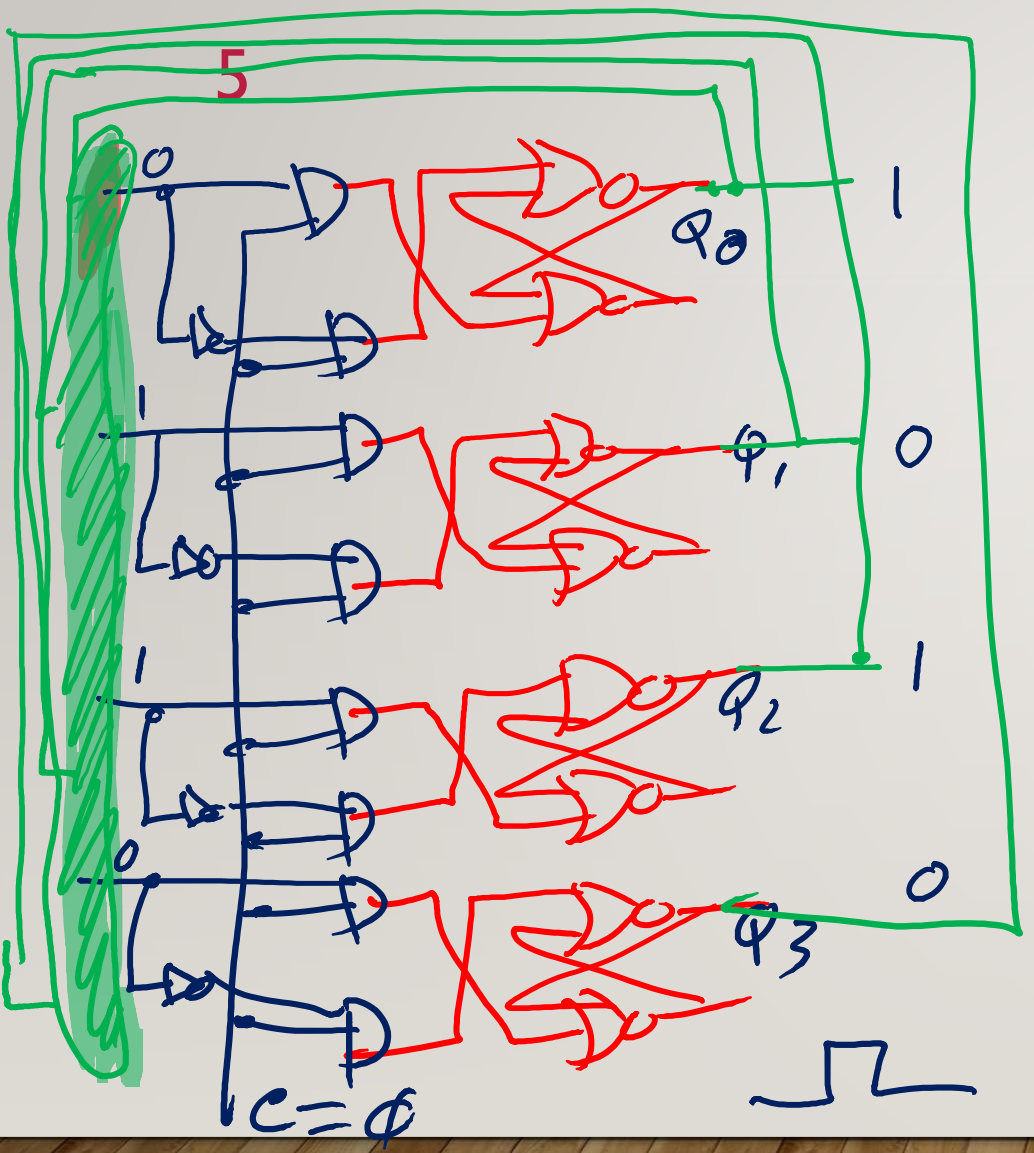

| C | S | R | $Q^+$ |
|---|---|---|---|
| ⎍ | 0 | 0 | Q |
| ⎍ | 0 | 1 | 0 |
| ⎍ | 1 | 0 | 1 |
| ⎍ | 1 | 1 | – |
| 0 | – | – | Q |

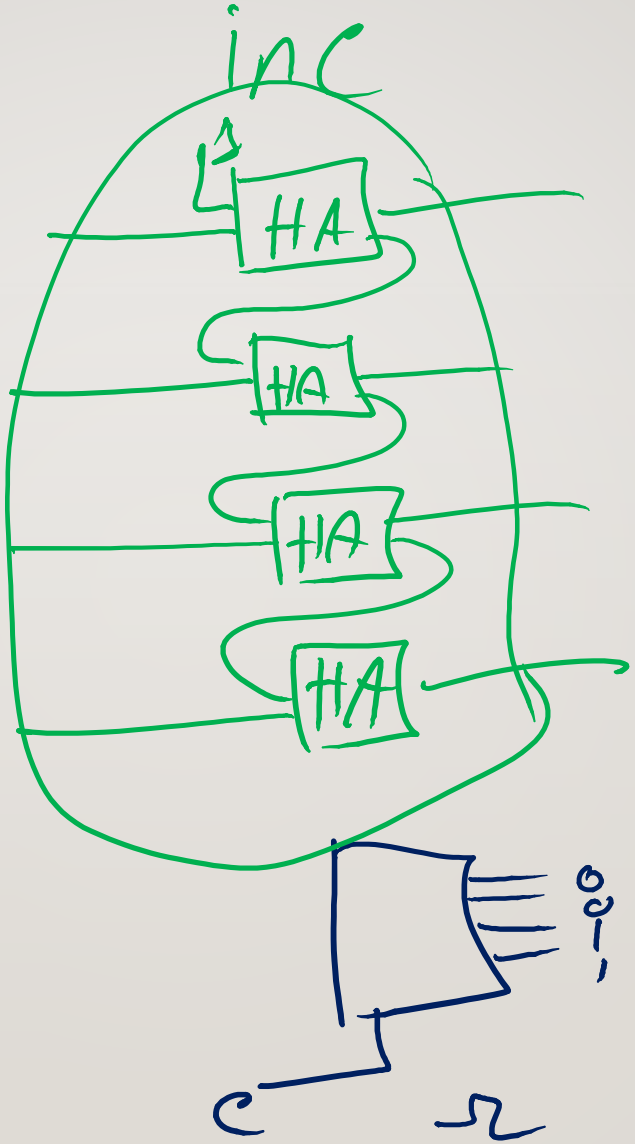


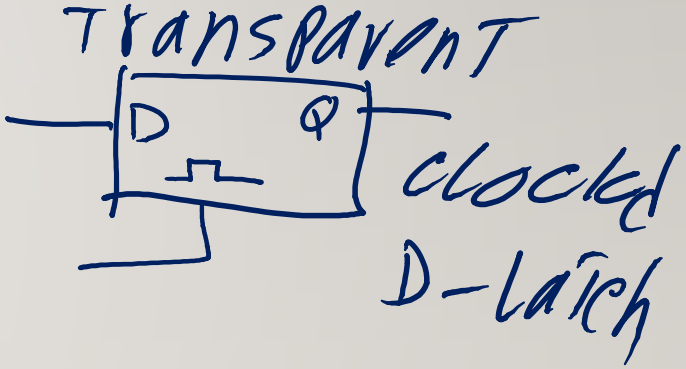

| C | D | $Q^+$ |
|---|---|---|
| ⎍ | 0 | 0 |
| ⎍ | 1 | 1 |
| 0 | – | Q |

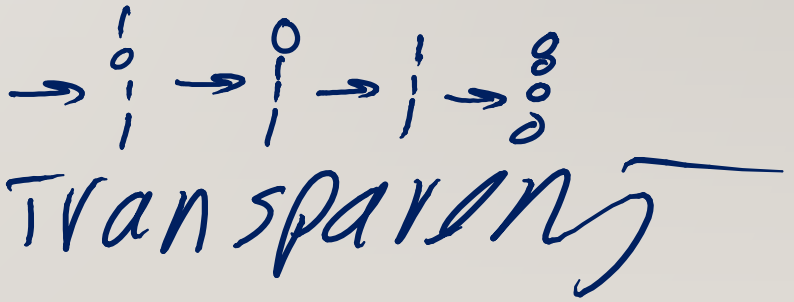
D-latch
Clocked D-latch
$Q^+ = D$

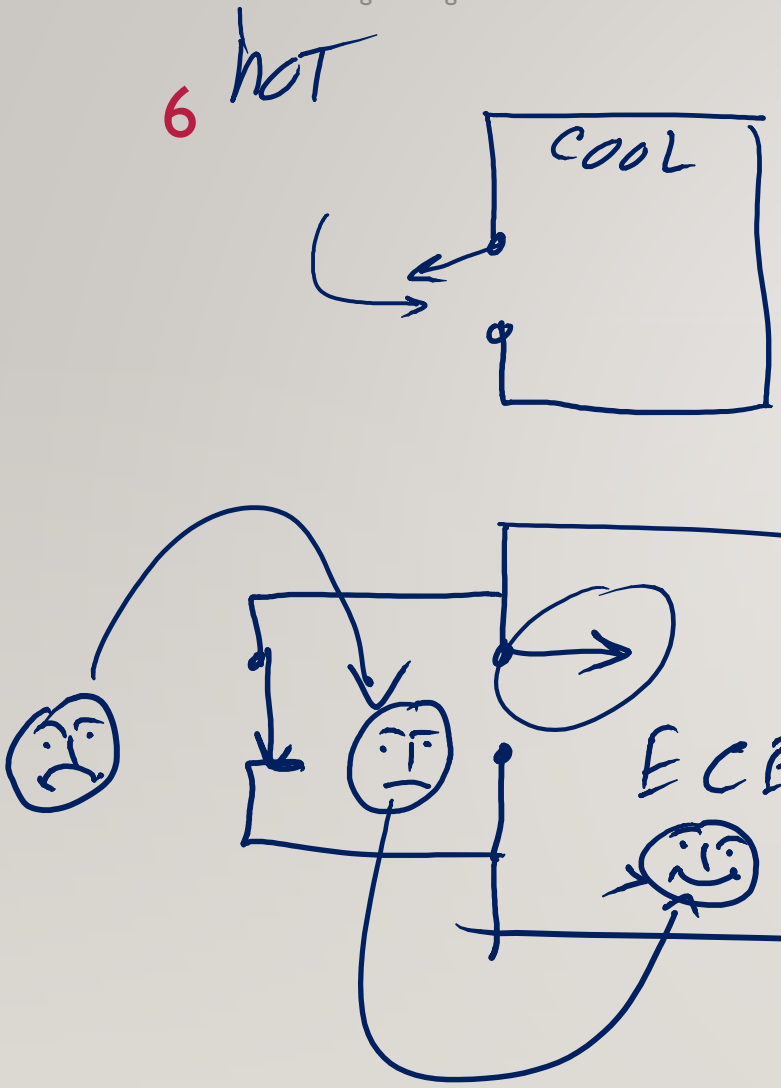
0 → 15

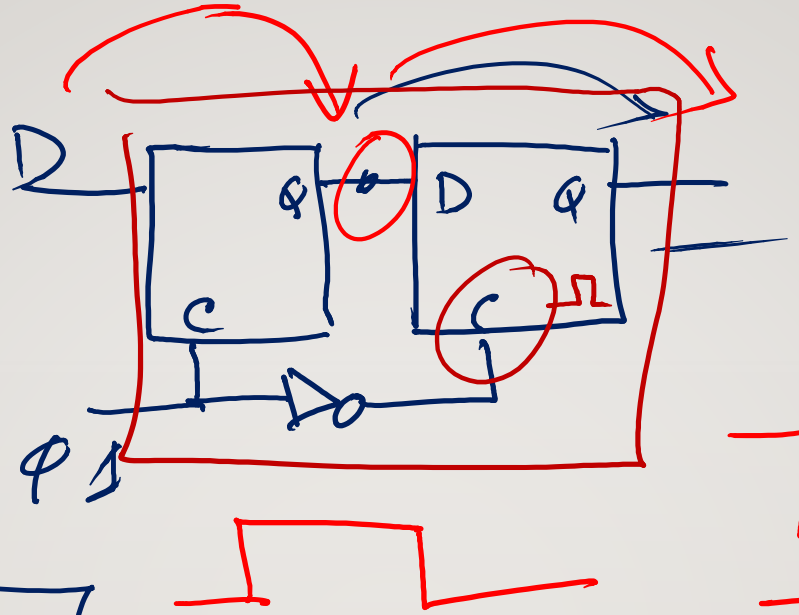

5
0
1
1
0
$Q_0$
$Q_1$
$Q_2$
$Q_3$
1
0
1
0
C=Φ

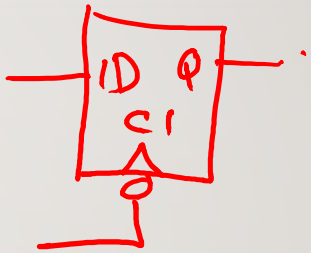

inc
1
HA
HA
HA
HA
C


Transparent
D
Q
clocked
D-latch

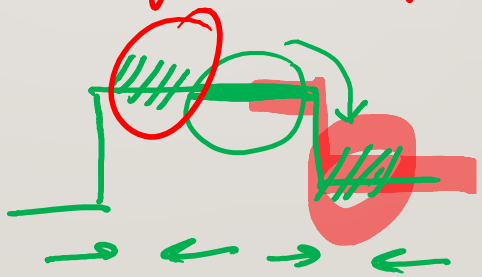

Transparent

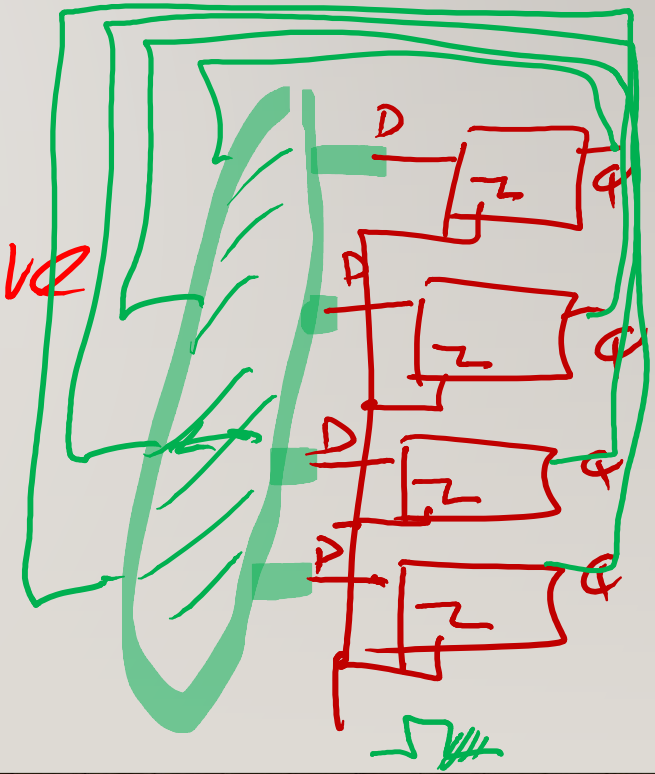


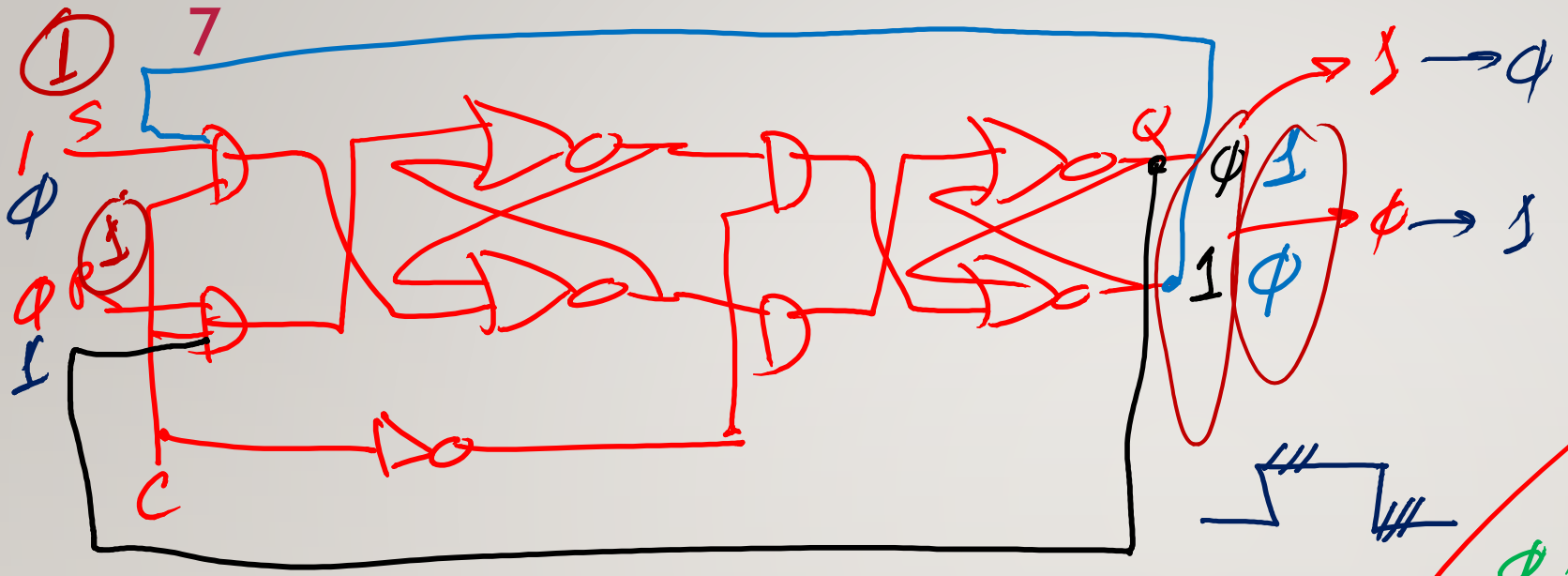




clocked Master-Slave D flip-flop





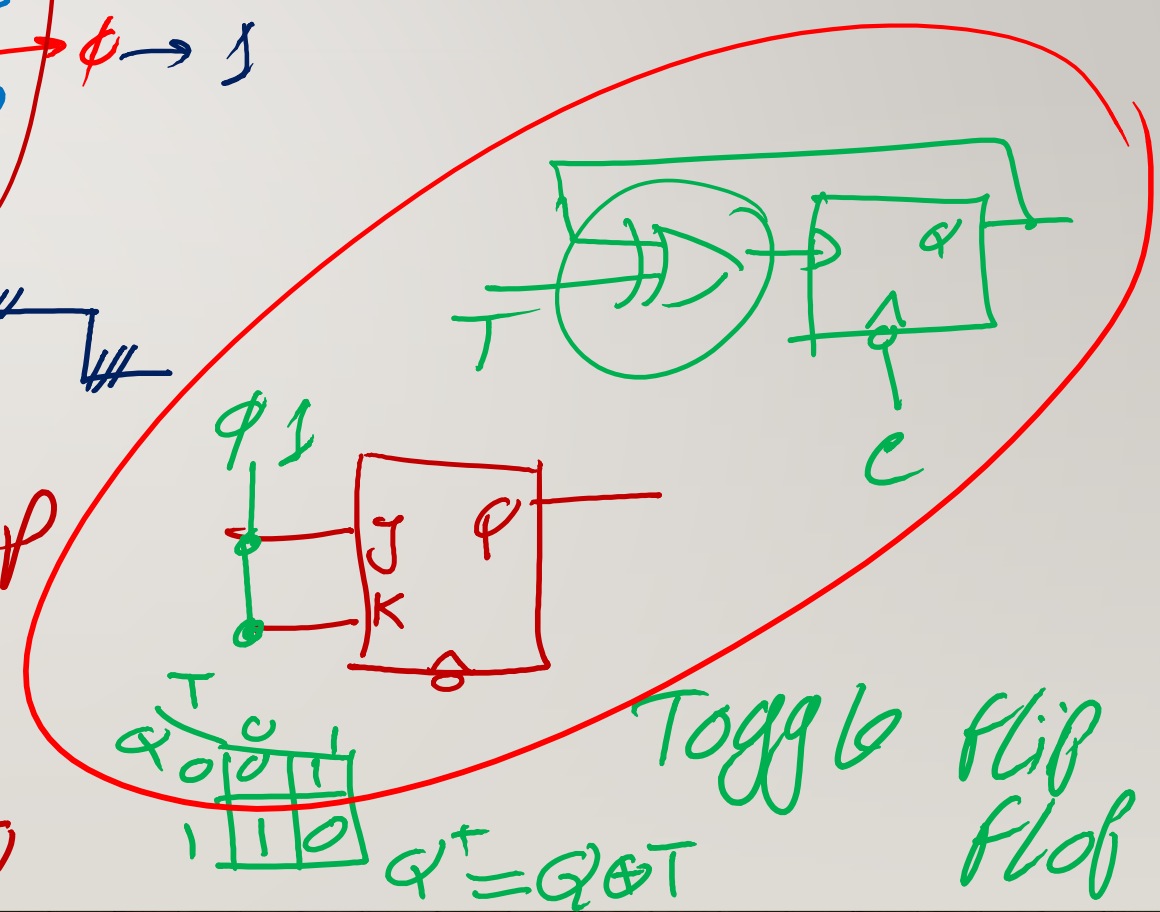



| C | J | K | $Q^+$ |
|---|---|---|---|
| 0 | 0 | 0 | $Q$ |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | $\bar{Q}$ |

JK Flip Flop

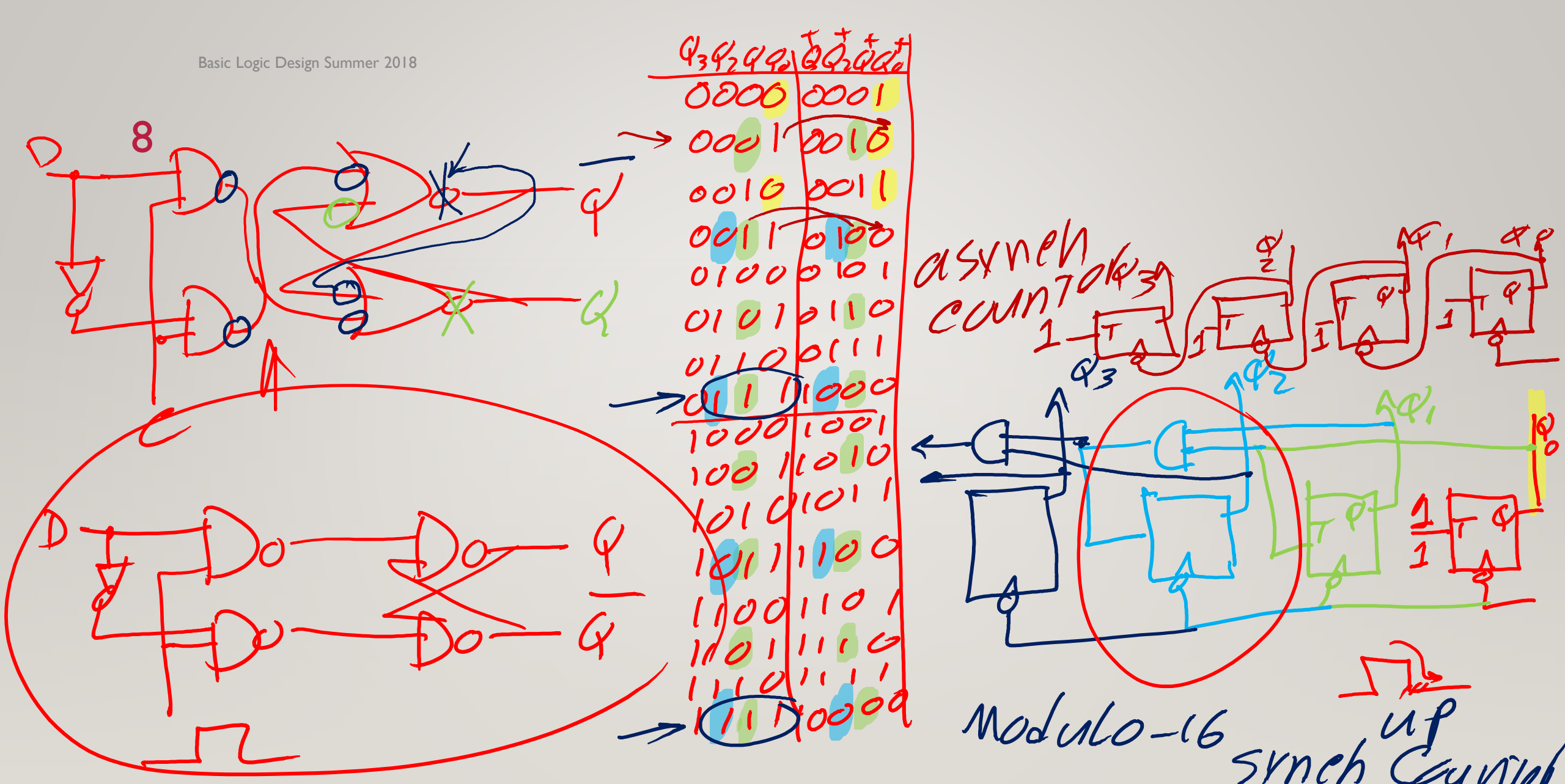
| JK / Q | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |

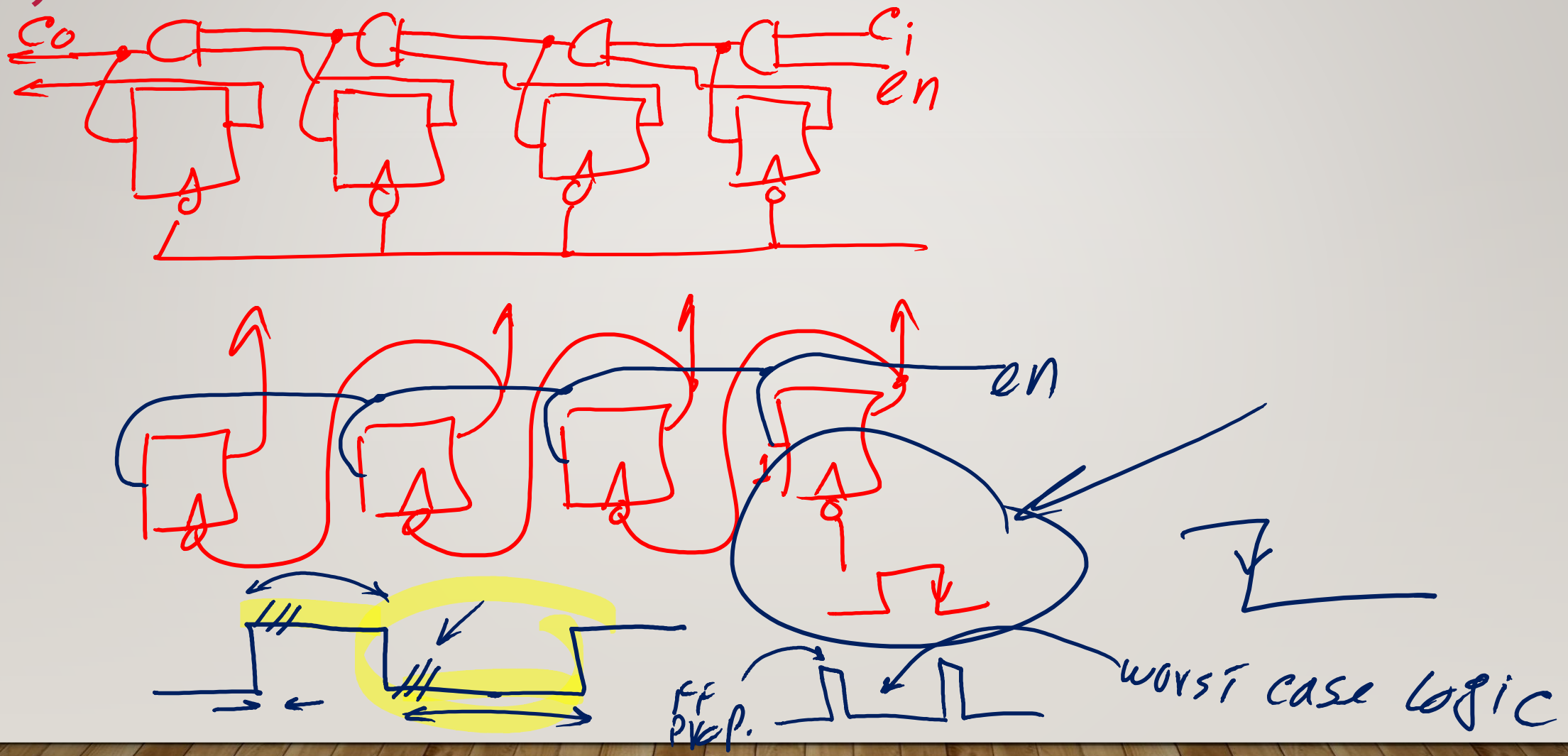
$Q^+ = J\bar{Q} + \bar{K}Q$

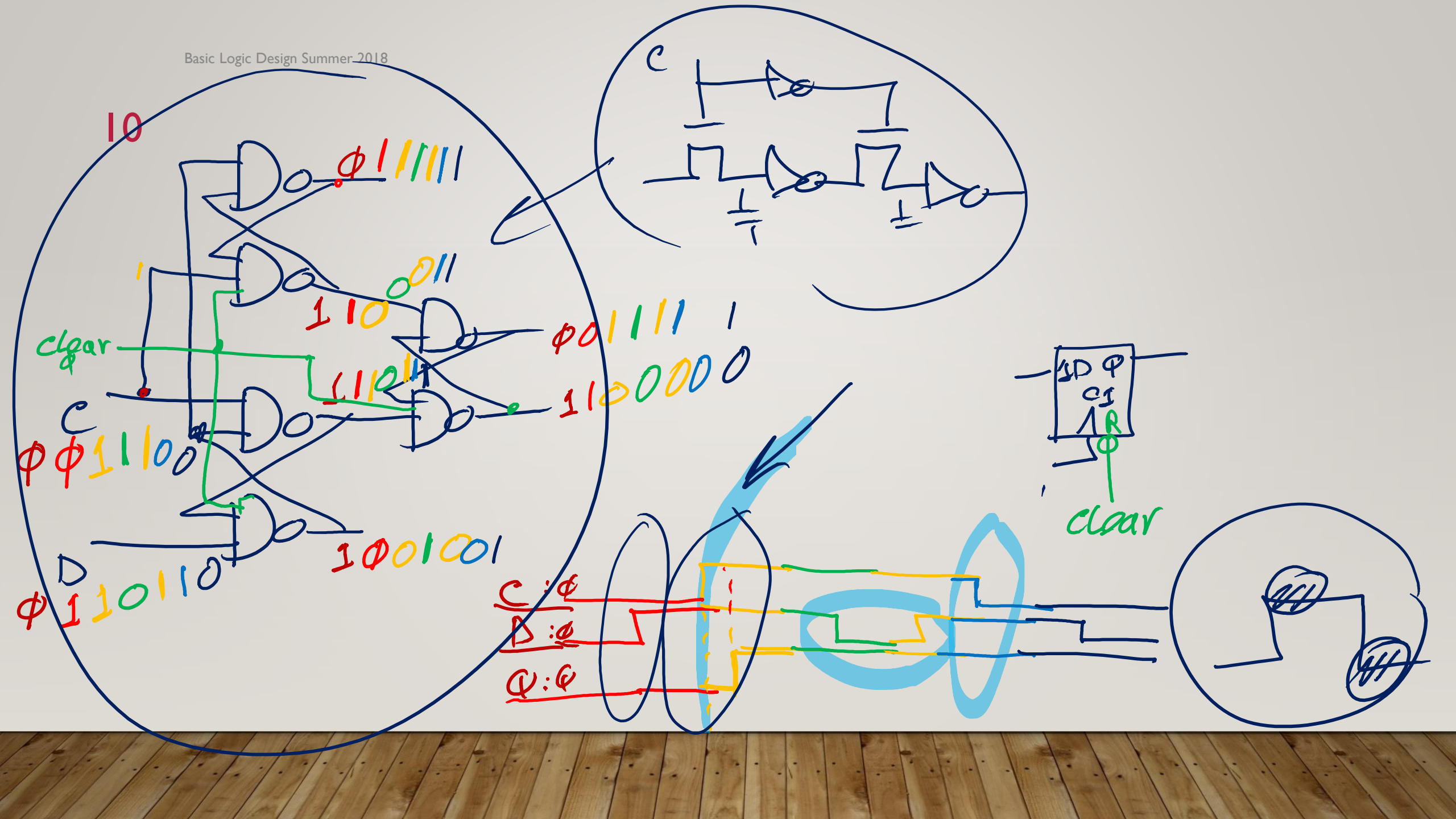



$Q^+ = Q \oplus T$

Toggle flip flop


8
asynch counter
Modulo-16
up
synch Counter


Co
Ci
en
en
worst case logic
FF
prop.


C
clear
D
clear

11