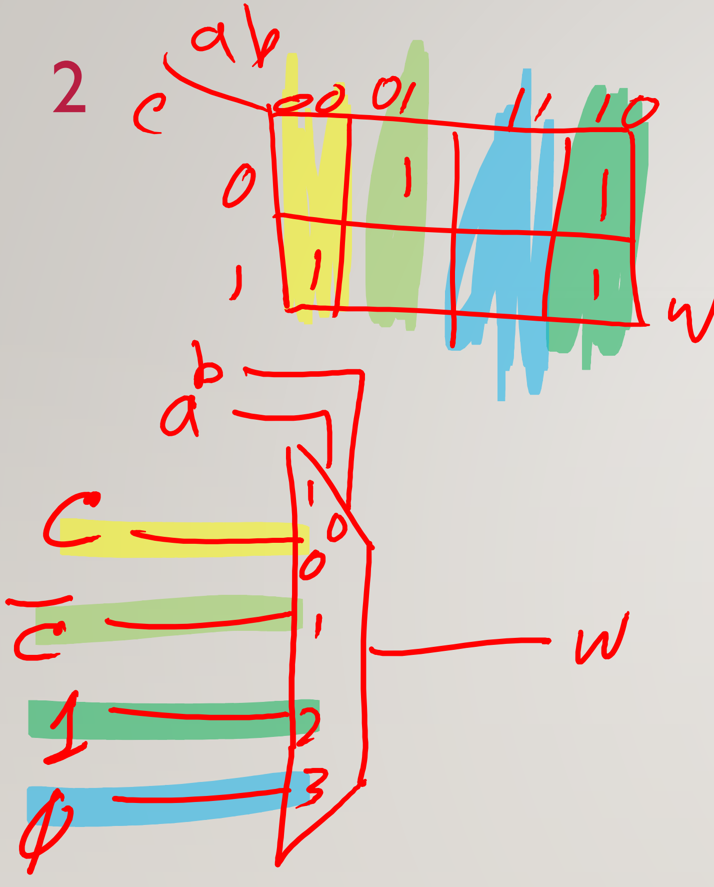
ICEEP
Iran Center of ESL Education and Promotion

Digital Logic Design

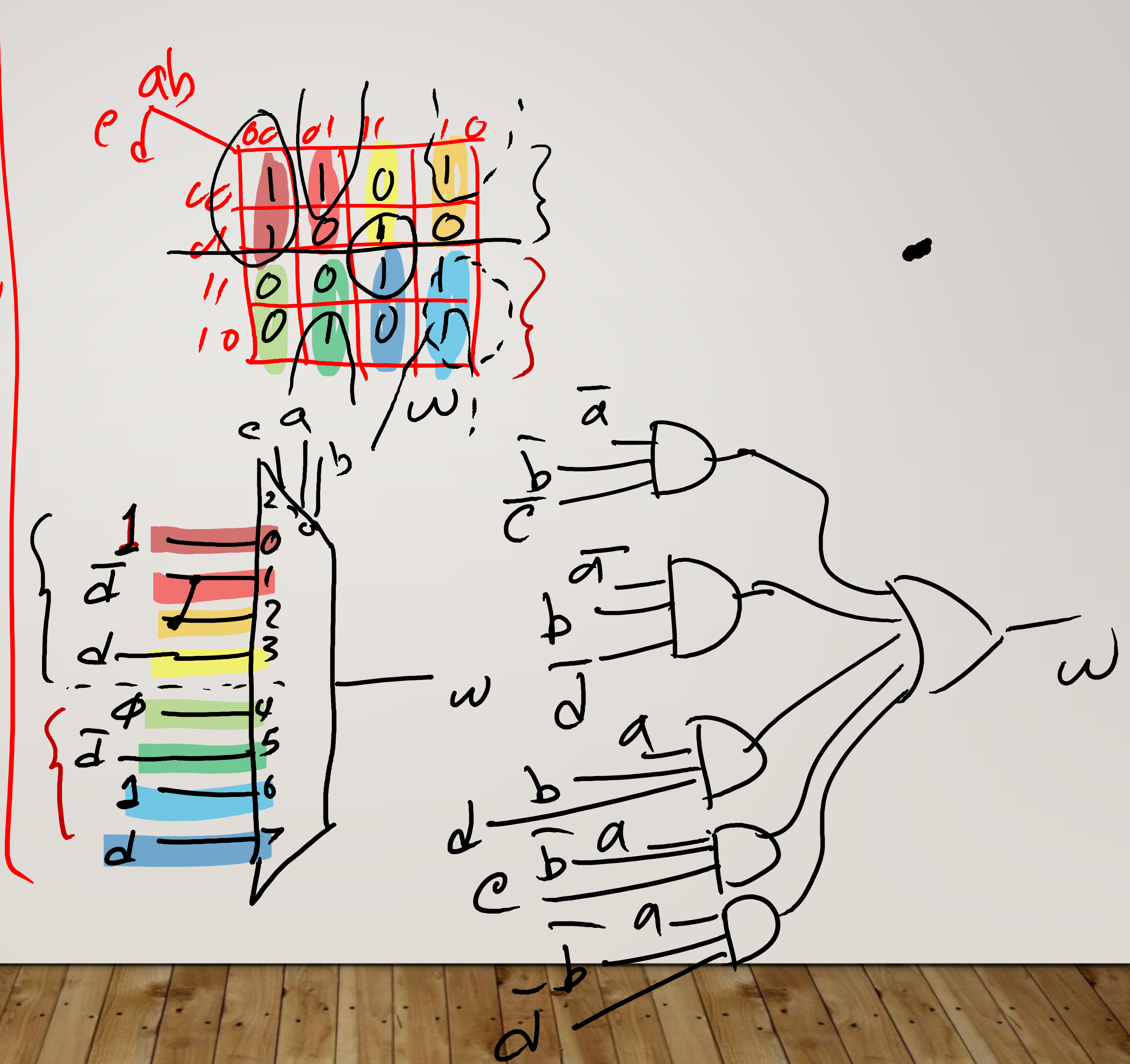
Lecture 6

Dr. Navabi

2

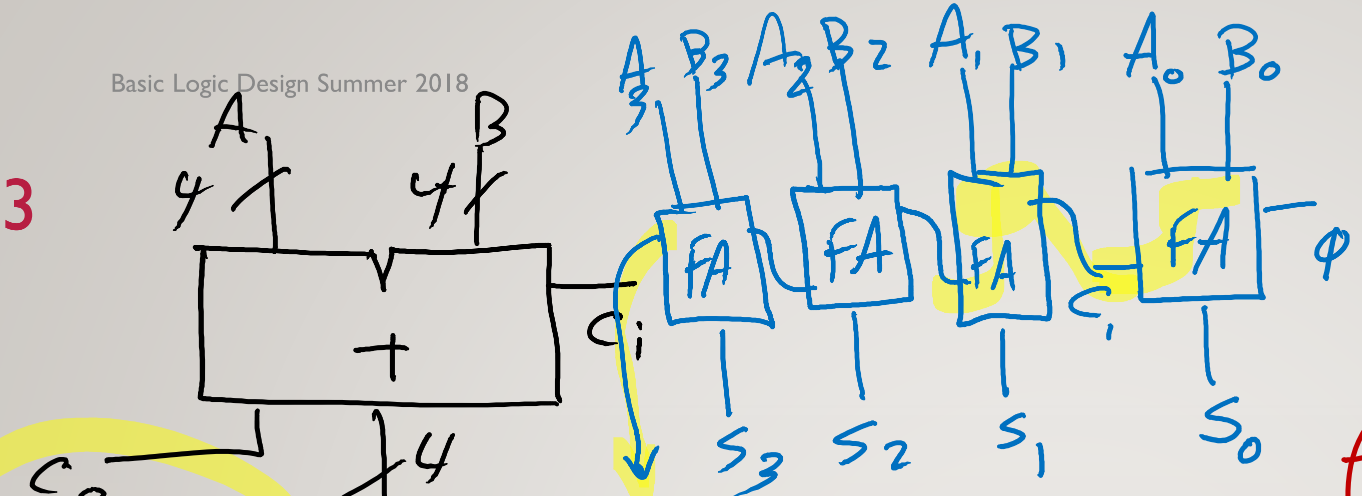


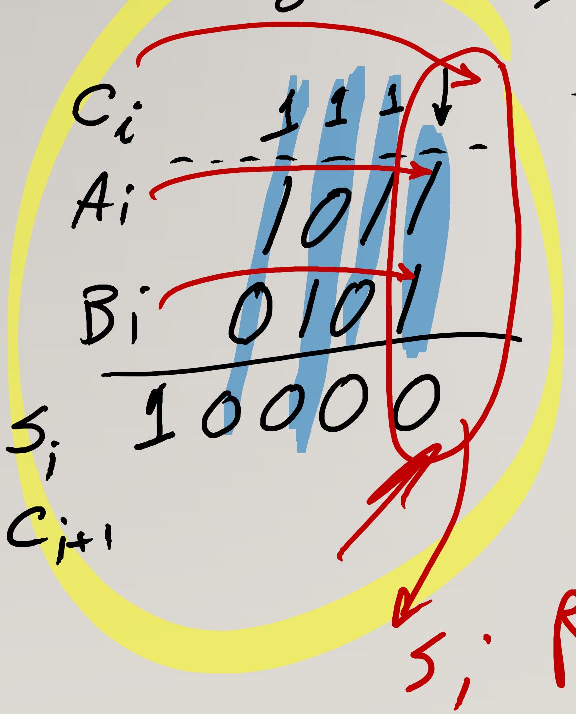
c \ ab	00	01	11	10
0		1		1
1	1			1



cd \ ab	00	01	11	10
00	1	1	0	1
01	1	0	1	0
11	0	0	1	1
10	0	1	0	1

3





RCA

$C_i A_i B_i$	C_o, S_i	
000	0	0
001	0	1
010	0	1
011	1	0
100	0	1
101	1	0
110	1	0
111	1	1

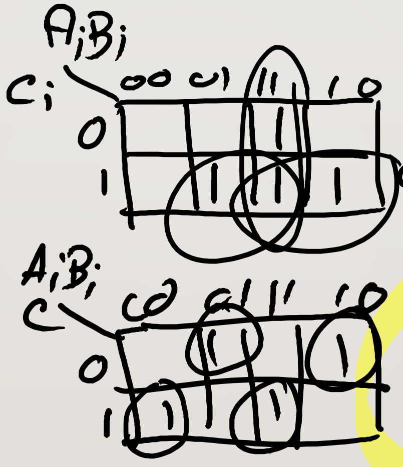
$c = C_i$

$a = A_i$

$b = B_i$

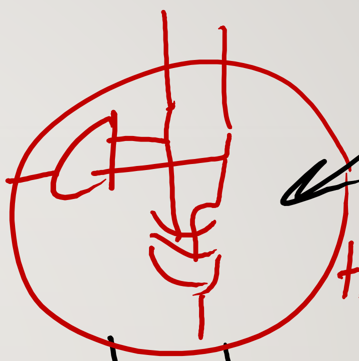
$s = S_i$

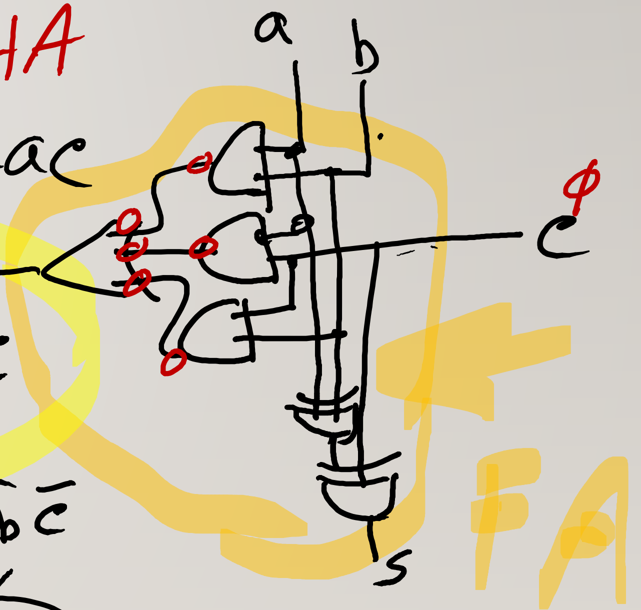
$c_o = C_{i+1}$



$C_o = ab + bc + ac$

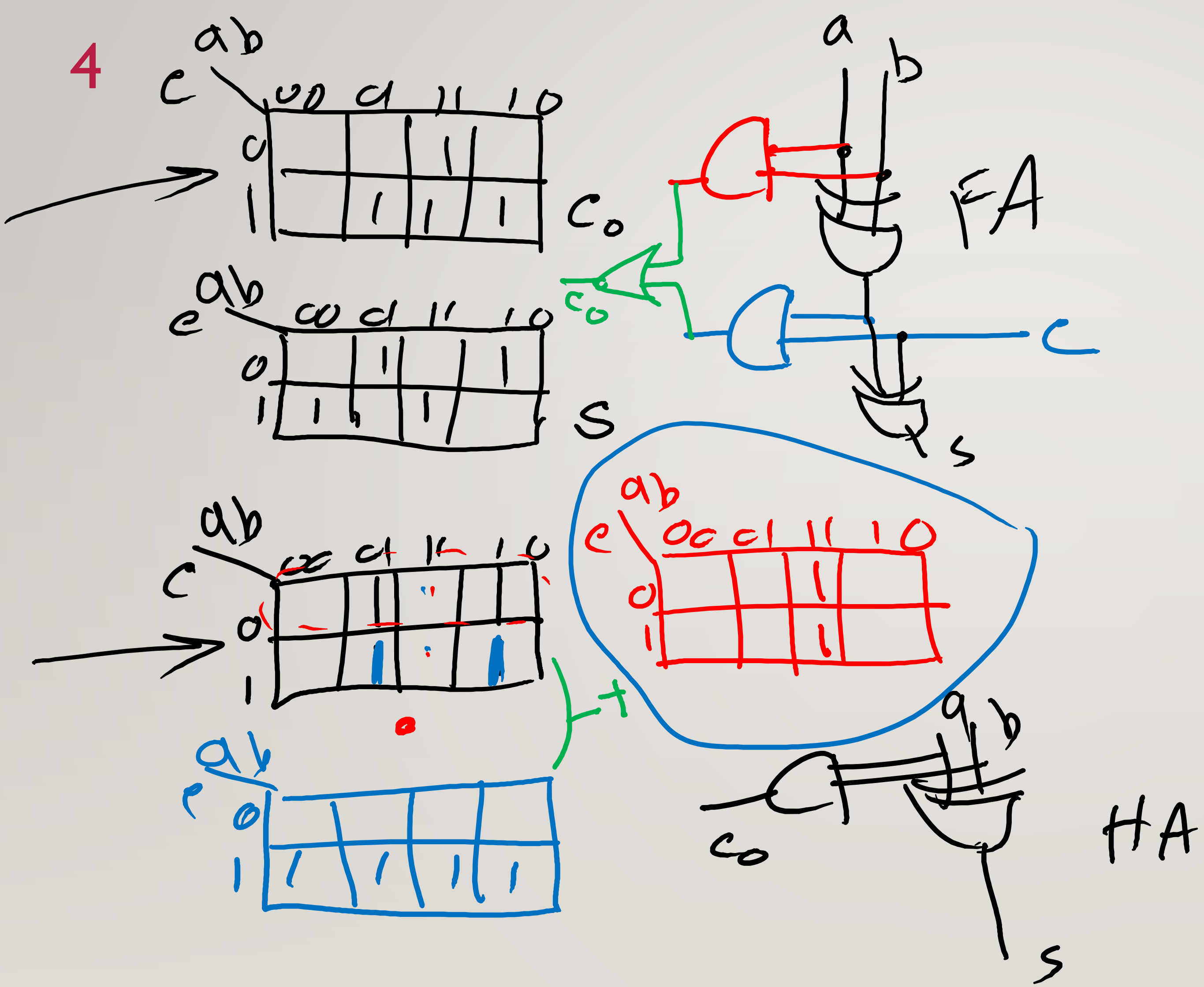
$S_i = a \oplus b \oplus c$


HA



$\bar{a} b \bar{c} + \bar{a} \bar{b} c + a b c + a \bar{b} \bar{c}$

$\boxed{\bar{a}}\underbrace{(b\bar{c} + \bar{b}c)}_{\boxed{b \oplus c}} + \boxed{a}\underbrace{(bc + \bar{b}\bar{c})}_{\boxed{\overline{b \oplus c}}} = a \oplus b \oplus c$



c \ ab	00	01	11	10
0			1	
1		1	1	1

Co

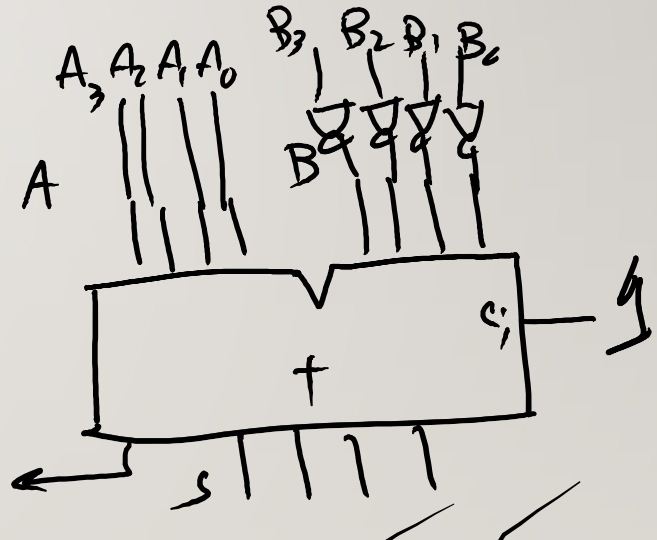
c \ ab	00	01	11	10
0		1		1
1	1		1	

S

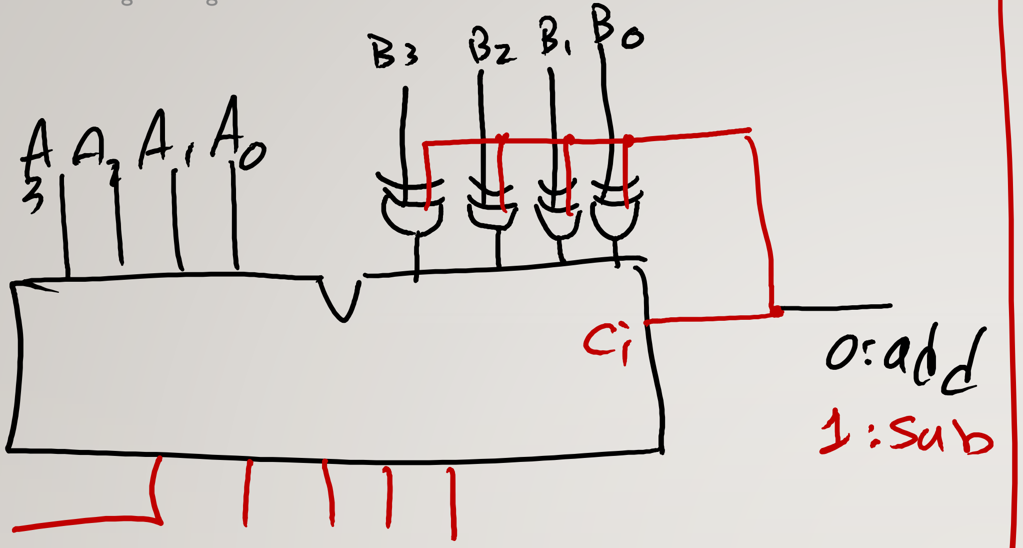
c \ ab	00	01	11	10
0				
1				

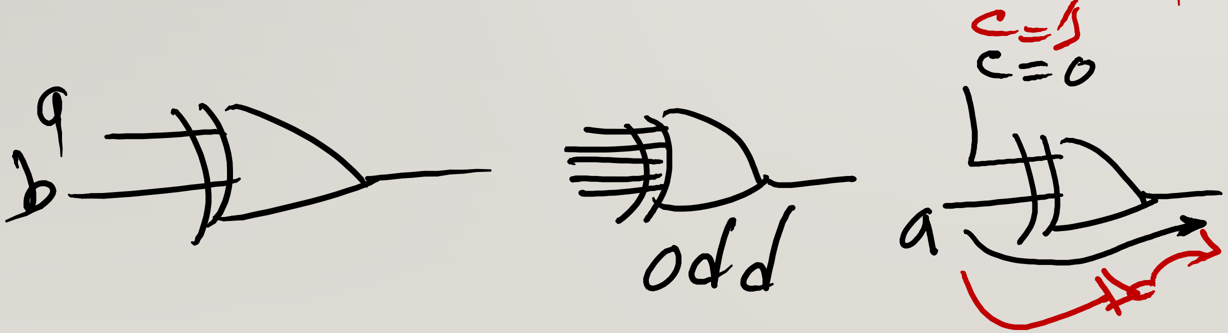
c \ ab	00	01	11	10
0			1	
1			1	

c \ ab				
0				
1	1	1	1	1

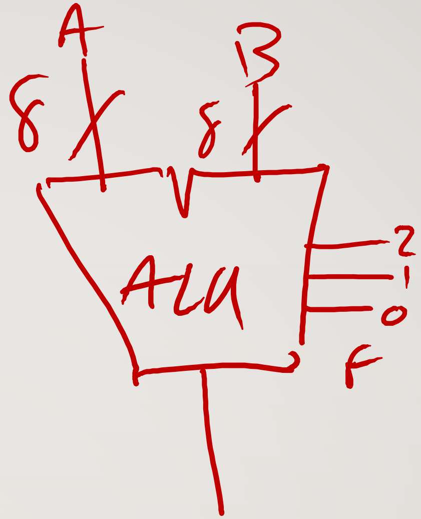


$$A - B = A + (\overline{B} + 1)$$

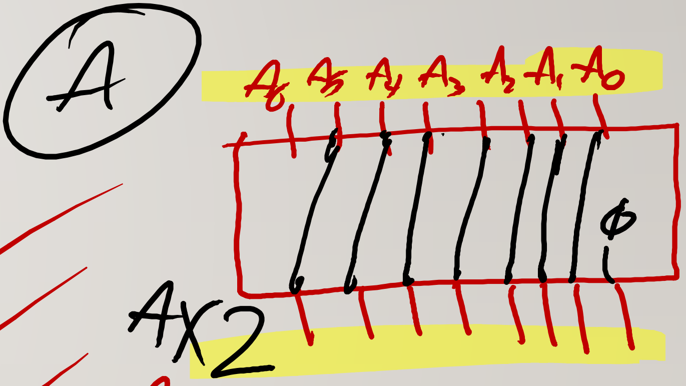




ALU



F	
0	A+B
1	A-B
2	A&B
3	A|B
4	A
5	A×2
6	A÷2
7	—



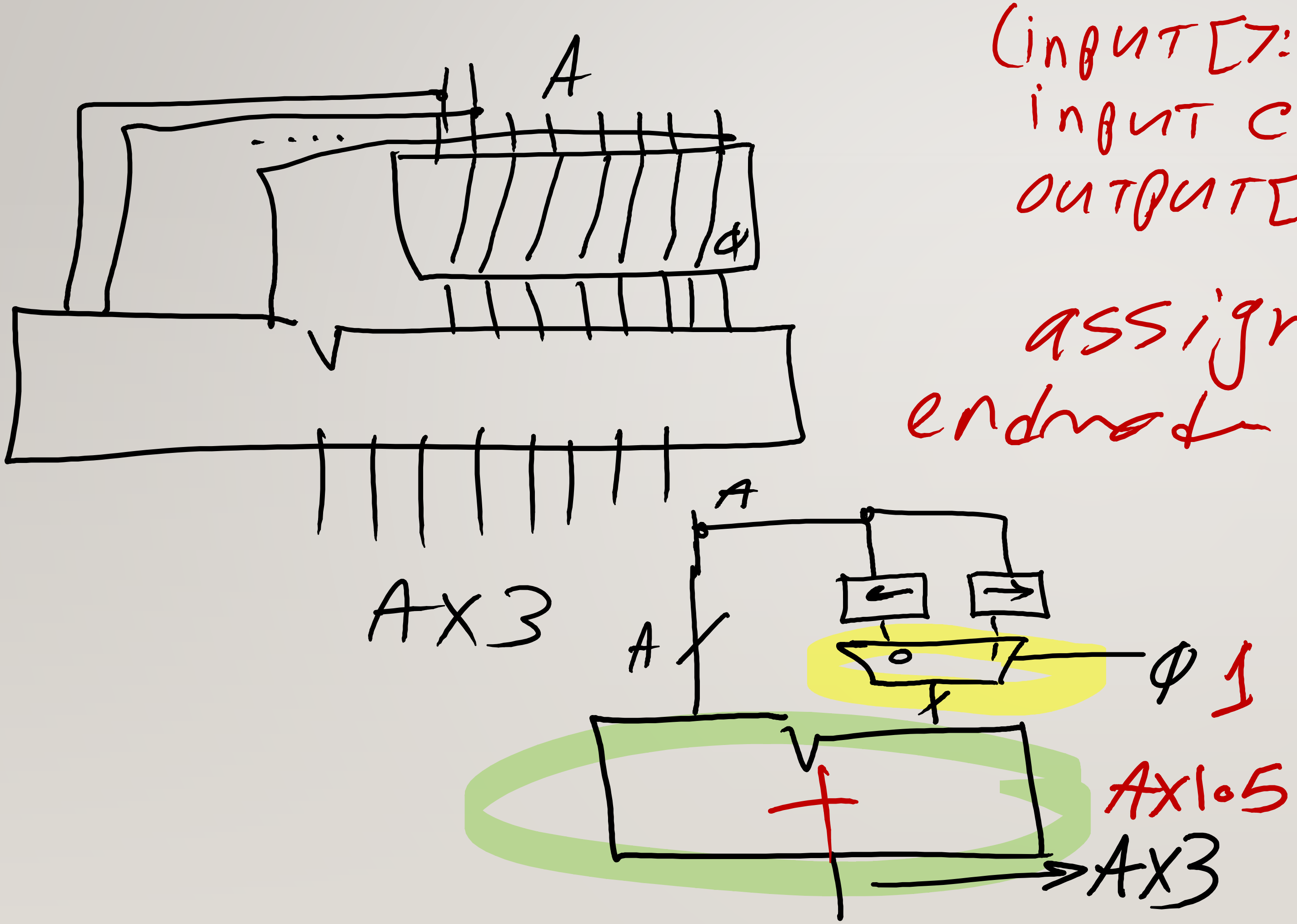
Arithmetic

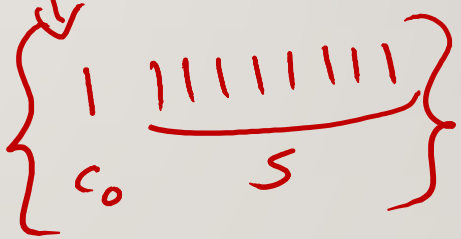
Logic

unit

```
module add8
    (input[7:0] A,B,
     input ci, output co,
    output[7:0] S);

    assign {co,s}=A+B+ci;
endmod
```



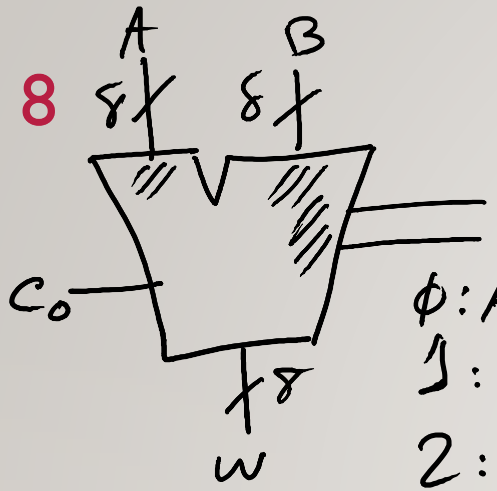


```
module FA(input a,b,c
      output reg co, s);
   assign {co, s} = a+b+c;
endmodu
```

```
#....
```

```
assign s = a⊕b⊕c;
assign co = a&b|a&c|b&c;
```

```
always@(a,b,c) begin
   {co,S}=a+b+c;
   ⋮
end
```



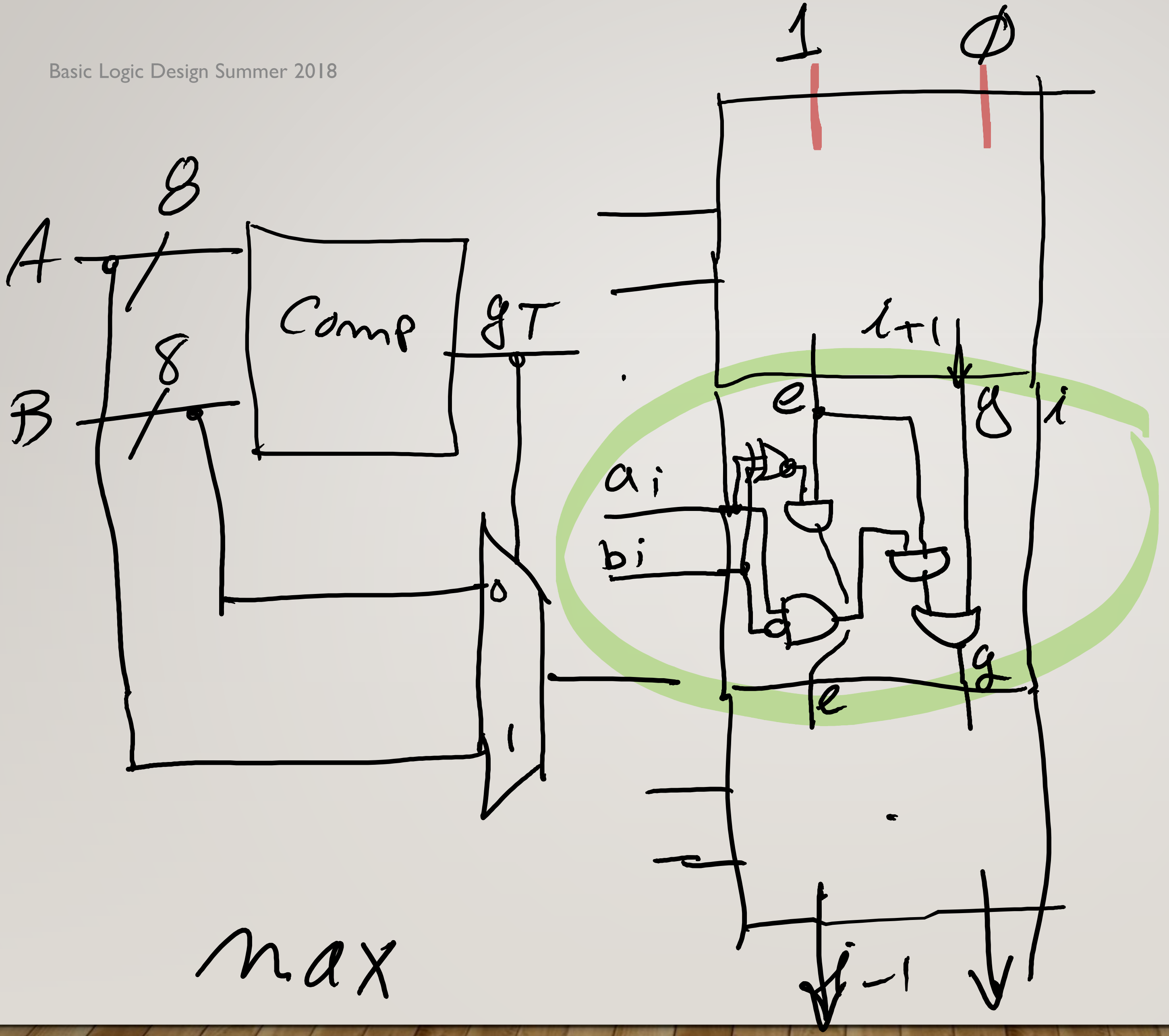
Ø: A+B
1: A+0.5B
2: Max(A;B)
3: A & B

1) Input Rule *
incle all signals
being read on the
always sensitiviy list

2) output Rule
indiscriminity sell all outputs to be
inactive values at
The beginig of
The always

```
module alu8(input [7:Ø] A,B, input [1:Ø] F,
    output reg co, output [7:Ø] reg w);
  always@(A,B,F) begin
    co = 1'bØ; w = 8'bØ;
    case (F)
    2'bØØ: {co,w} = A+B;
    2'bØ1: co,w} = A+0.5B
    2'b1Ø: if (A>B) w=A; else w=B;
    2'b11: w= A & B;
    default: w= 8'bØ;
```

```
endcase
end
endmodule.
```



1 1 0 1
1 0 1 1
1 0

A: 1 1 1 Ø
B: 1 1 0 1
3 2 1 0