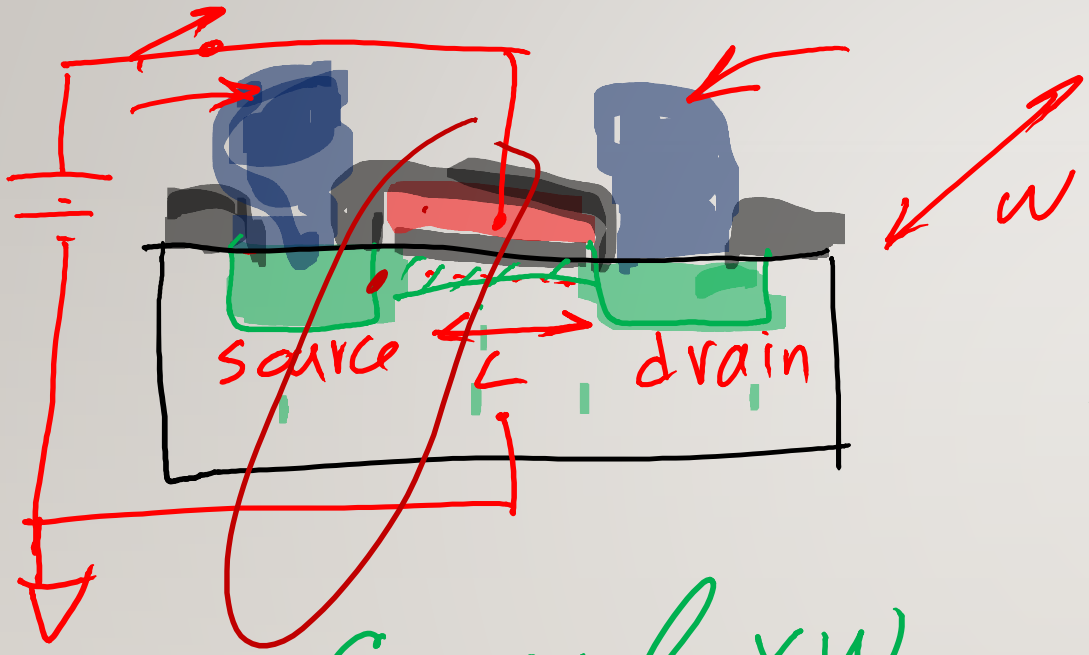
ICEEP
Iran Center of ESL Education and Promotion

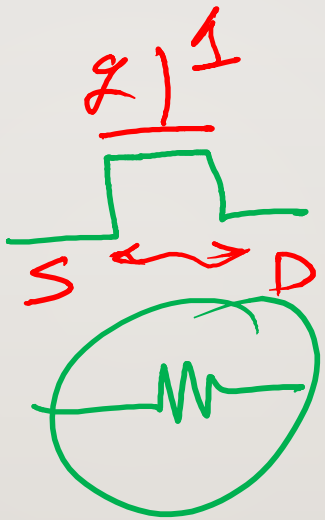
# Digital Logic Design

## Lecture 2

**Dr. Navabi**

# 2 Transistors

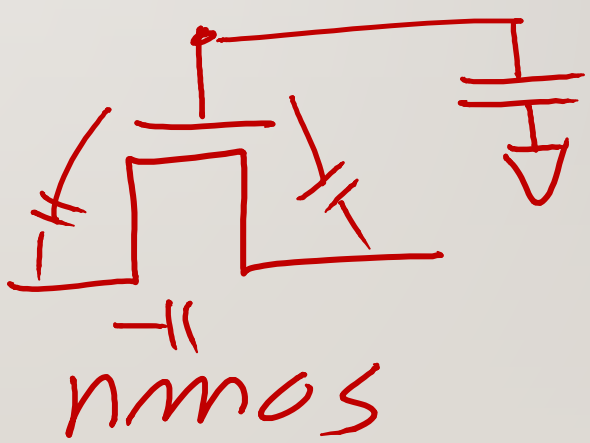


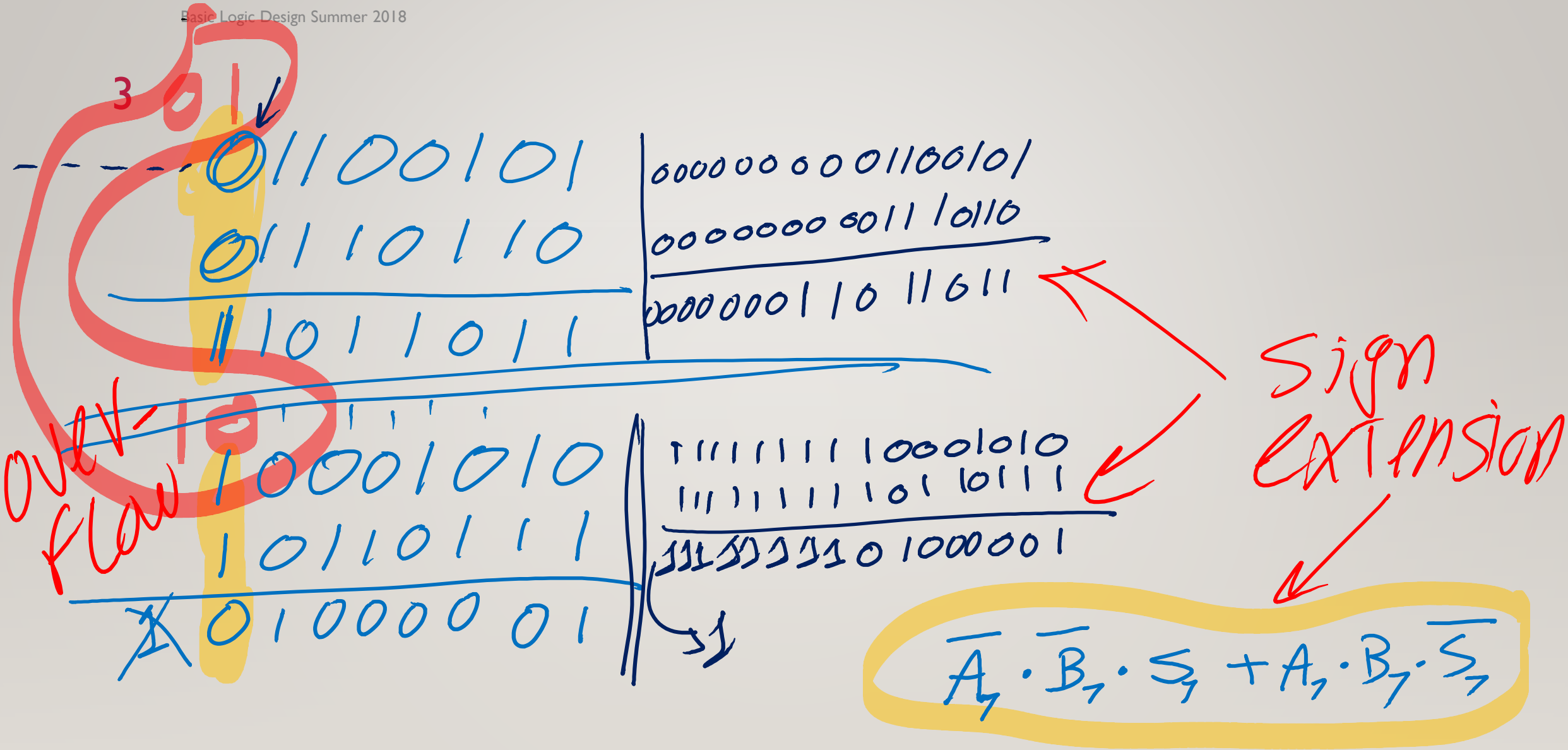





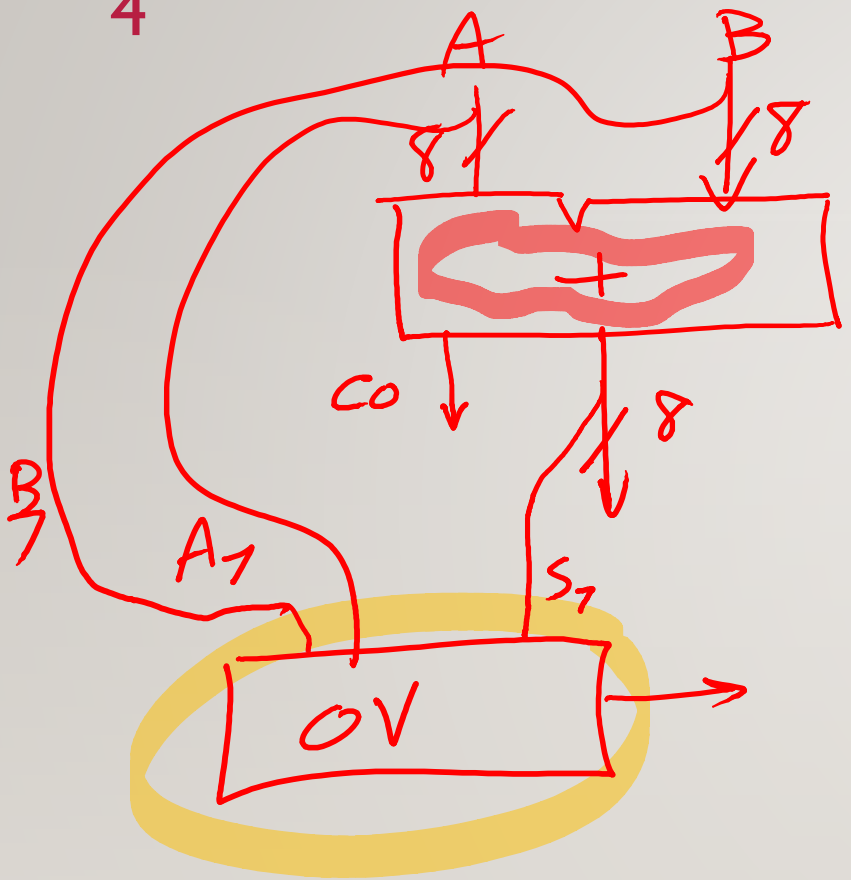
$C_g \sim l \times w$

$R_g \sim l/w$



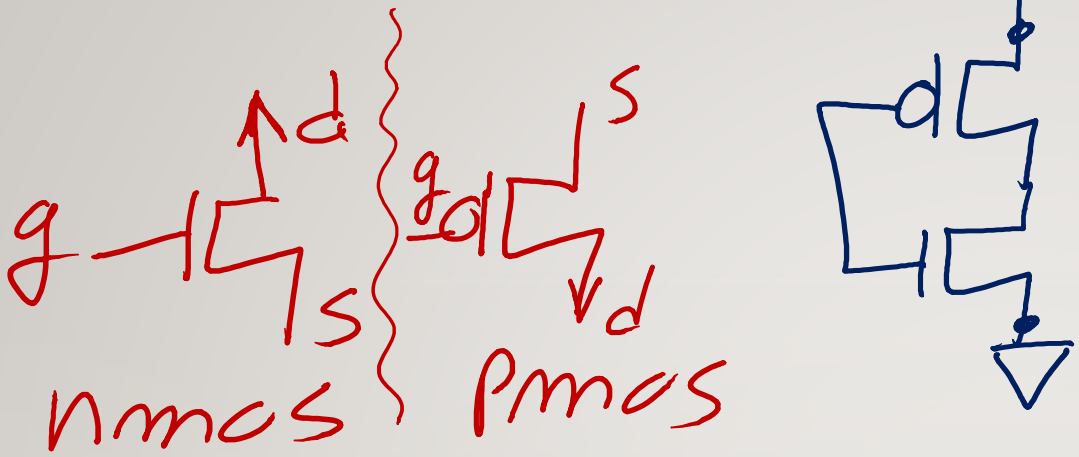


3
0 1 1 0 0 1 0 1
0 1 1 1 0 1 1 0
1 1 0 1 1 0 1 1
0000000001100101
0000000001110110
0000000110 1101 1
overflow
1 0 0 0 1 0 1 0
1 0 1 1 0 1 1 1
1 0 0 0 0 0 0 1
1111111110001010
1111111101011111
1111111101000001
sign extension
$\overline{A_7} \cdot \overline{B_7} \cdot S_7 + A_7 \cdot B_7 \cdot \overline{S_7}$

4




overflow detector

5







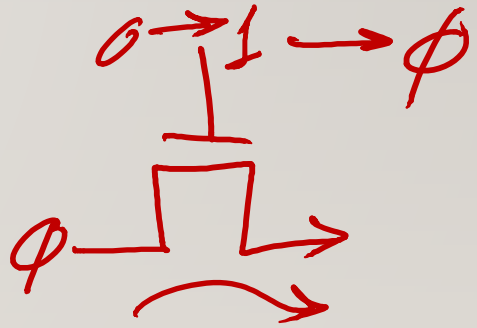
nmos #(3,5,7) (d, s, g);

pmos #(5,7,9) (d, s, g);

#5
#7

| 0 | 1 | Z | X |
|---|---|---|---|

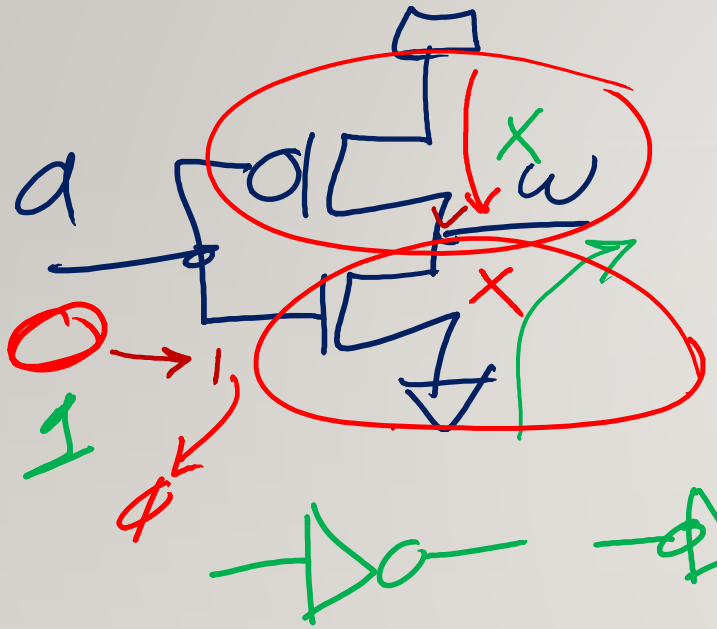
TO1, TOφ, TOZ



6

# Build Inverter

| a | w |
|---|---|
| 0 | 1 |
| 1 | ϕ |



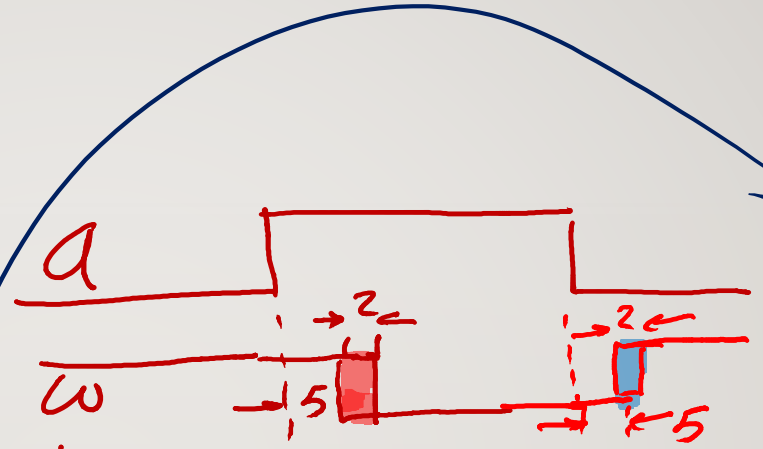



$w = \overline{a}$

$= \neg a$

$= \sim a$

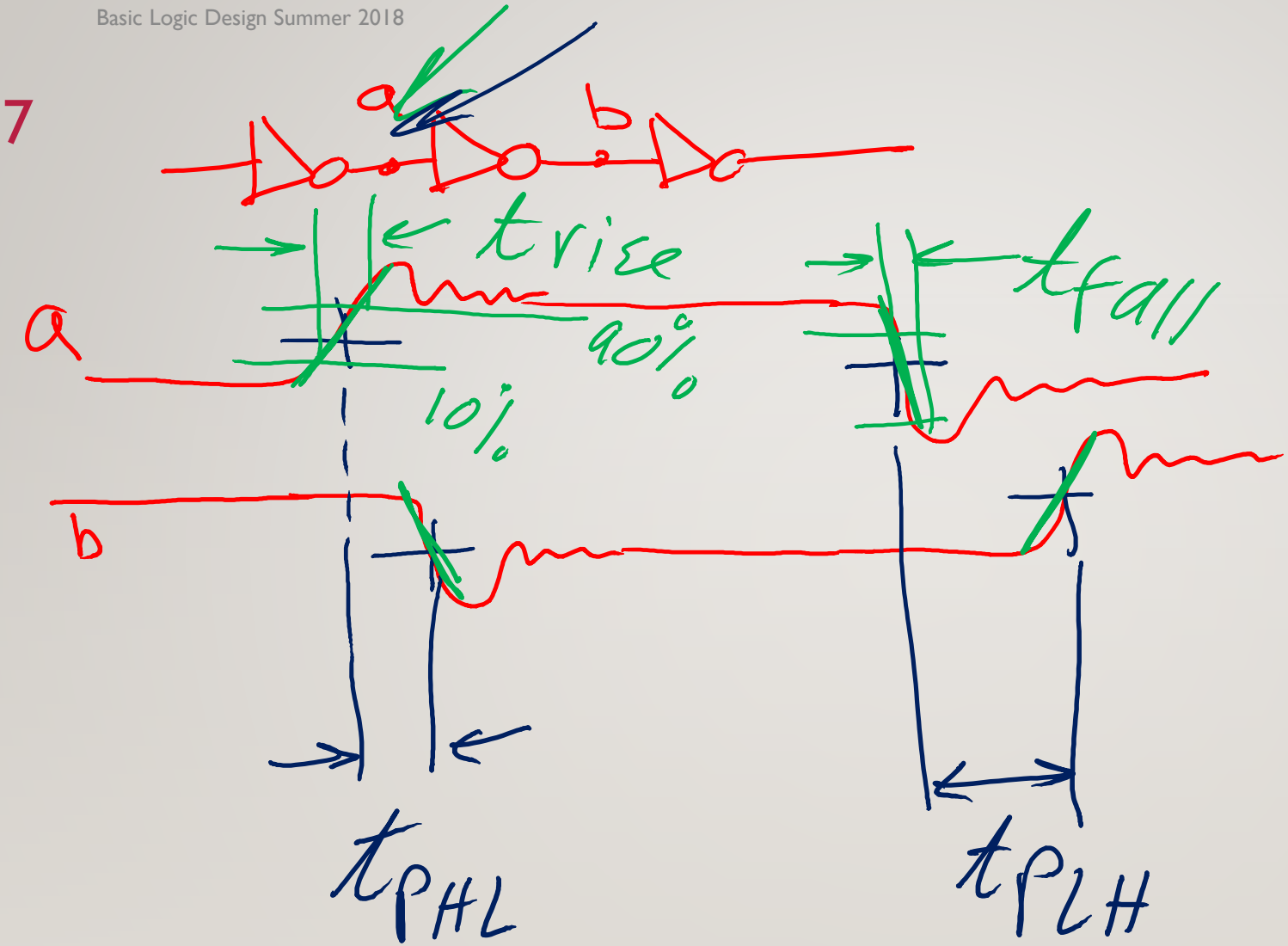
```
not #7(w,a);
```

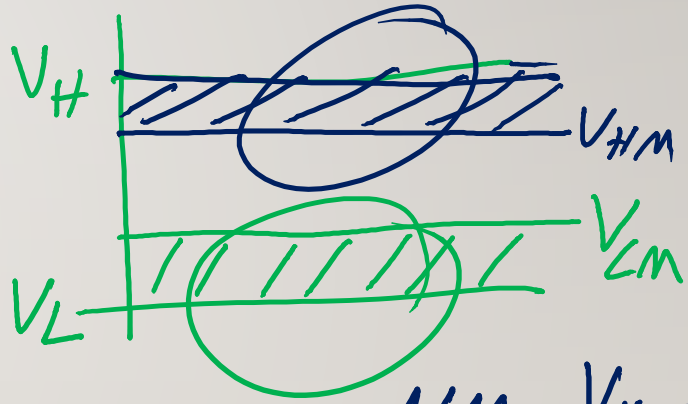



```
module myinv (input a, output w);
  supply1 Vdd;
  supply0 Gnd;
  pmos #7 (w,Vdd,a);
  nmos #5 (w,Gnd,a);
endmodule
```

CMOS

WORST CASE : 7

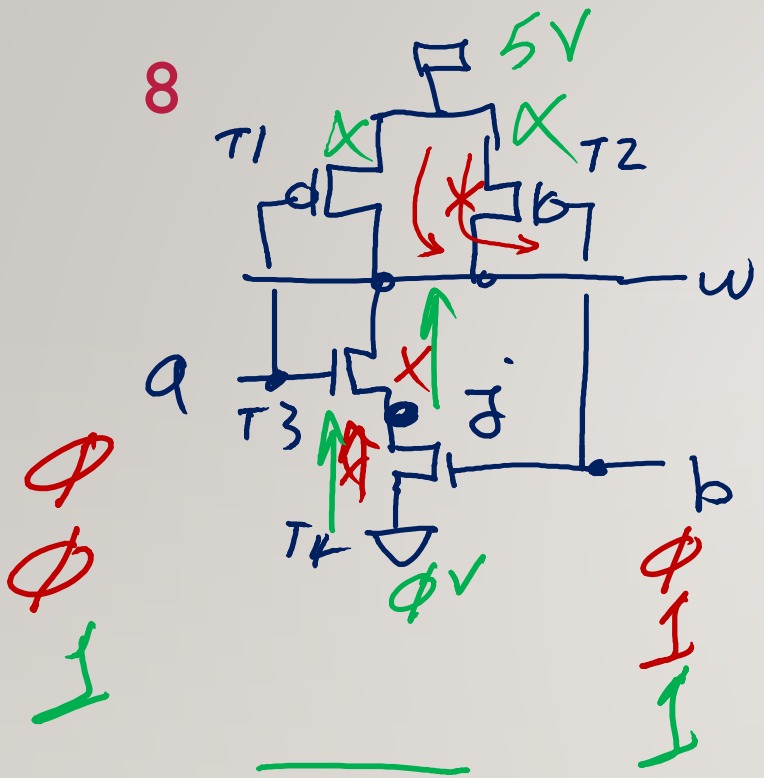



$$NM = \frac{V_{HM} + V_{LM}}{2}$$

$$t_d = \frac{t_{PLH} + t_{PHL}}{2}$$

8




| a | b | w |
|---|---|---|
| φ | φ | 1 |
| 0 | 1 | 1 |
| 1 | φ | 1 |
| 1 | 1 | 0 |


NAND

$$w = \overline{a \cdot b}$$
$$= a \uparrow b$$
$$= \sim(a \& b)$$

#10
nand #(10,8) (w,a,b);

```
module mynand(inputa,b,
                              output w);
  wire y;
  supply1 Vdd;
  supply0 Gnd;
  pmos #7 T1(w,Vdd,a);
  pmos #7 T2(w,Vdd,b);
  nmos #5 T4(y,Gnd,b);
  nmos #5 T3(w,y,a);
endmodule
```