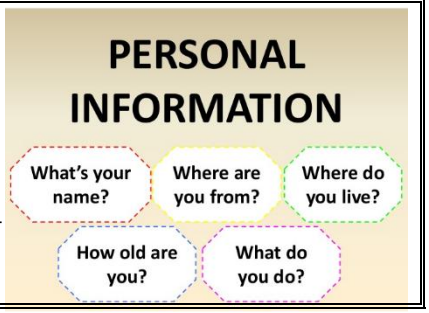
UNIVERSITY OF TEHRAN
Electrical and Computer Engineering
ECE (8101) 432

Object Oriented Modeling of Electronic Circuits
Spring 93-94
Final Exam

Computer Account#_____

First Name:_____; Last Name:_____

Student Number:_____; Signature:_____



Grade:

Problem 1. _____/20

Problem 2. _____/20

Problem 3. _____/20

Problem 4. _____/20

Total: _____/100

Takhte-Soleyman (Near Zanjan). Zoroastrian temple (Sassanid), Mosque (Ilkhanian)

DO NOT USE LAPTOPS
EXTRA SHEETS WILL NOT BE ACCEPTED
YOU MUST SHOW COMPLETE WORK ON ALL PROBLEMS
YOU HAVE EXACTLY 150 MINUTES FOR WORKING ON THIS TEST
A ONE-PAGE INFORMATION SHEET (CHEAT SHEET) IS ALLOWED

SystemC RTL

1. Show the design of a sequential circuit for calculating *n*-factorial, where *n* is an 8-bit integer, and the result is a 16-bit integer. The circuit has a 1-bit *get* input, an 8-bit *nBus* input, a 1-bit *completed* output, and a 16-bit *nfBus* output. When *get* is 1, the 8-bit data will be read from the *nBus* and factorial calculation begins. When completed, a one-clock duration pulse will be placed on completed output. When a factorial calculation is completed the circuit looks at get again and if it is still 1, it will pick up the next n and run calculations again. With the get and completed signals behaving as described, a device requiring factorial calculation can place different *n* inputs on the *nBus* without having to wait for an elaborate handshaking. Synchronizing reception of a result and placement of the next n is the task of the factorial requesting device. Since in many cases, factorial calculations are to be done for consecutive numbers, our factorial calculation device always keeps the information about its most recent calculation, and if the next calculation is for a number above the previous calculation, it can calculate the new factorial in just a few steps without having to start from 1.

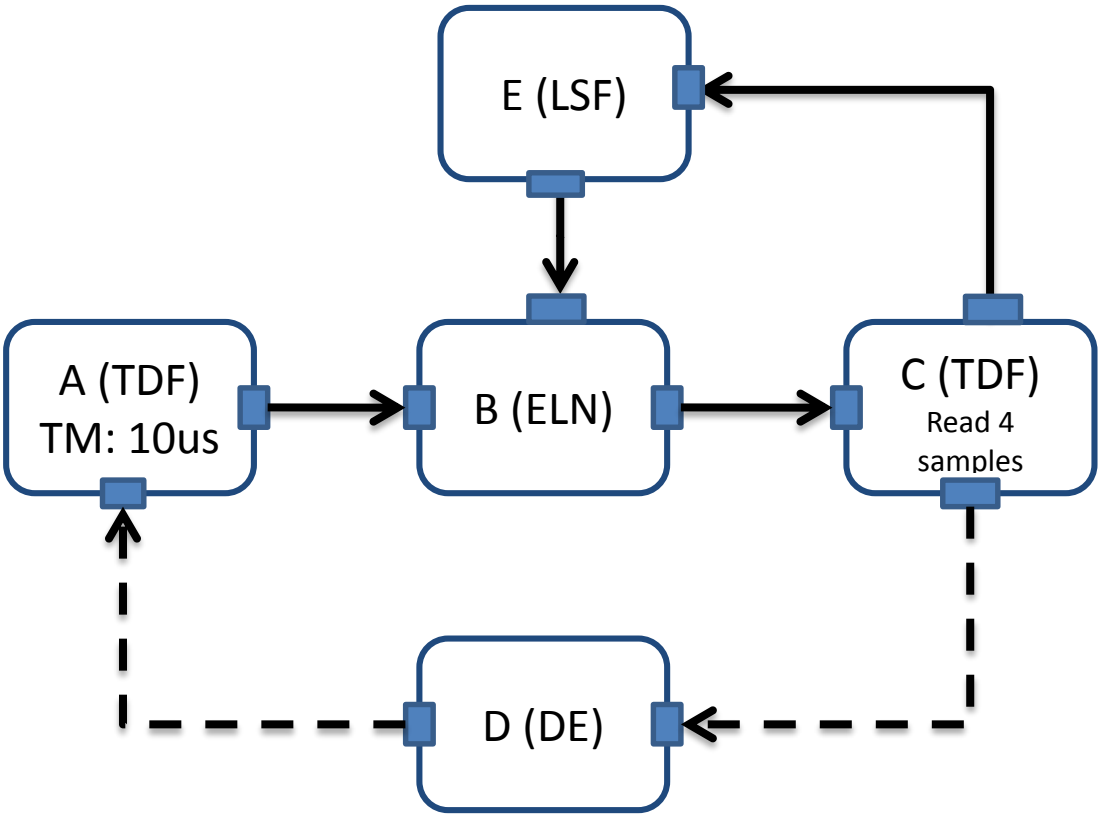
   A) Show the complete datapath of this circuit. Show its block diagram using RT level components. Clearly indicate the control signals.
   B) Show the controller.
   C) Wire the datapath and control unit in an SC_MODULE, write a SystemC testbench module to initialize and test several master-slave communications of this system.
   D) Write an sc_main for instantiating and testing this RTL design.

SystemC Linguistics

2. The *sc_semaphore* protocol can be used for arbitration of a shared device between several master modules. In this problem you will have to model five master modules wanting to access a fictitious device that allows only four simultaneous accesses. For this purpose, you are to use a semaphore of size 4. SystemC descriptions are required. Write five SystemC SC_MODULE master modules that connect to an *sc_semaphore*. Each module requests the use of the fictitious device at random times and uses the device for a random amount of time before it is done with it. Each master module prints the time it requests the use of the device, reports (prints) if it was granted the permission to use the device, and reports the time it releases the device. Write codes for the modules such that there will be times that the semaphore cannot respond to a request because all its tokens are taken. Simulate and write activities to an activity file.

SystemC-AMS Design

3. System shown below is to model in a mixed signal environment. The system is constructed form five modules that are implemented in different modeling formats (DE, LSF, TDF and ELN).
   - **A.** Define a time step of 10 US for module A. Define a time step for all ports and modules of the system. Define rate and delay attributes for the ports, if needed. Define a scheduling for this system.
   - **B.** Show the prototype of each module in this system, (defining modules, ports and mandatory functions).
   - **C.** Connect all modules together in an SC_MODULE and construct the complete system. Specify ports, signals, module binding and type of ports and signals.



SystemC-AMS Modeling

4. Write ELN module for the transfer function of the following circuit in SystemC-AMS. Use the same rates for input and output. Input of this module is from a digital circuit and its output goes to an analog module that is modeled with a LSF module.